



MASS manufacturing of TrAnsceiverS for Terabit/s era

Deliverable D7.1 Factsheet and project presentation

Programme:	H2020-ICT-2018-2
Project number:	825109
Project acronym:	MASSTART
Start/End date:	01/01/2019 - 31/12/2021

Deliverable type:	Report
Deliverable reference number:	825109/ D7.1/ V.1
Deliverable title:	Factsheet and project presentation
WP contributing to the deliverable:	WP7
Responsible Editor:	Fraunhofer Fraunhofer IZM Gustav-Meyer-Allee 25 13355 Berlin, Germany
Due date:	28/02/2019
Actual submission date:	28/02/2019

Dissemination level:	Public
Revision:	FINAL



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Abstract: The deliverable contains the factsheet and brief presentation of the project.

Keywords: Factsheet, project description



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Abbreviations

PIC	Photonic Integrated Circuits
I/O	Input/Output
TSV	Thorough Silicon Via
PSM4	Parallel Single Mode 4-channel
QFSP-DD	Quad Small Form-factor Pluggable double density
DP-64QAM	Dual polarization 64 Quadrature amplitude modulation
WDM	Wavelength Division Multiplexing



1 Executive Summary

This document contains the factsheet of the MASSTART project alongside a brief description of the project's goals.

2 Introduction

2.1 Purpose of this document

This document contains the factsheet of the MASSTART project alongside a brief description of the project's goals.

2.2 Document structure

The present deliverable contains the following chapter:

- ❖ Factsheet

2.3 Audience

This document is public.

3 Factsheet



MAIN OBJECTIVES

MASSTART aims to provide a holistic transformation to the assembly and characterization of high speed photonic transceivers towards bringing the cost down to €1/Gb/s or even lower in mass production. This will guarantee European leadership in the Photonics industry for the next decade. MASSTART will surpass the cost metric threshold by using enhanced and scalable techniques:

- i) glass interface based laser/PIC and fiber/PIC coupling approaches, leveraging glass waveguide technology to obtain spot size and pitch converters in order to dramatically increase optical I/O density, while facilitating automated assembly processes
- ii) 3D packaging (TSV) enabling backside connection of the high speed PIC to a Si carrier
- iii) a new generation of flip chip bonders with enhanced placement in a complete assembly line compatible with Industry 4.0 which will guarantee an x6 improvement in throughput
- iv) wafer-level evaluation of assembled circuits with novel tools that will reduce the characterization time by a factor of 10, down to 1 minute per device.

DEMONSTRATORS

This process flow will be assessed with the fabrication and characterization of four different demonstrators, addressing the mid-term requirements of next generation transceivers required by Data Center operators and covering both inter- and intra- Data Center applications. These demonstrators are:

- i) a 4-channel PSM4 module in QSFP-DD format with 400G aggregate bit rate
- ii) an 8-channel WDM module in a QSFP-DD format with 800G aggregate bit rate,
- iii) a 16-channel WDM on-board module delivering 1.6Tb/s aggregate line rate
- iv) a tunable single-wavelength coherent transceiver with 600Gb/s capacity following the DP-64QAM modulation format on 64Gbaud/s line rate.

Finally, MASSTART will interact closely with international bodies to ensure the compliance and standardization of the developed technology with other proposed packaging form factors for rapid commercialization.

AMBITION

The main advantages of Silicon Photonics technology to build optoelectronic data transmission modules is its ability to address high complexity devices and high manufacturing volumes by leveraging CMOS manufacturing process and equipment, at the noticeable exception of specific building blocks (particularly optical interconnect of the optical fibers). However, there is presently no high maturity level products combining these two characteristics:

- In one hand, high complexity devices (switches, Network On Chip, etc...) remains limited to R&D demonstrations, at TRL 4.
- In another hand, commercial devices like 400Gb/s transceivers remain limited in term of number of implemented optical functions and form factor

MASSTART aims at addressing these two challenges, by building a design,

manufacturing and test process first, but also by pushing the full integration flow at TRL7 and having an active role within standardization committees. Indeed, this development will be led by choosing the best strategies in order to reduce the module overall cost by:

- Improved automation of packaging process and test
- Introduction of new wafer level manufacturing steps to enhance circuit and module performances (SiN layer, TSVs)
- Use of scalable techniques such as the WAFT technology for fiber and laser assembly that relax alignment tolerances

Reducing transceiver cost is driving the datacom and telecom industries as a result of the cost reduction effort carried out by the DC operators. The COGS for a singlemode transceiver such as the 400G and 800G devices described here, is influenced mostly by:

- i) PIC cost
- ii) alignment cost.

For a dedicated Si process fab costs can go well below 1€/mm² for high volume production. For the cost of a PIC it is important to distinguish between chip cost and packaged module cost, as for now the cost of a PIC is only a small part of the total cost of a module, as the assembly and packaging are dominant cost factors and are addressed in the MASSTART project.

The second cost factor is alignment cost; in silicon photonic transceivers, there are two such processes: laser coupling to the PIC and fiber coupling to the PIC. Both require high alignment accuracy as the PIC waveguide dimensions are very different from both the laser waveguide and the fiber.

IMPACT

MASSTART directly addresses the specific challenge of ICT-04-2018, topic Photonics based manufacturing, access to photonics, datacom photonics and connected lighting, through its following

expected impacts. It will reduced manufacturing cost of PIC-based optical transceivers with transfer rates above 1Tb/s enabling massive deployment in datacenter environments (<1€/Gb/s between racks and <0.1€/Gb/s inside rack).

MASSTART fact sheet

Grand Agreement: 825109

Duration: Jan 2019 - Dec 2021 (36 Months)

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Total Budget: € 7 476 435 Euros

EC contribution: € 5 999 936,25 Euros

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