PICs for data center interconnect

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virtual conference session:

Data Center Interconnects – Towards Mass Manufacturing

online / October 6th 2020 / 4 - 7pm



PICs for data center interconnect

Benjamin Wohlfeil 6.10.2020



Company overview



Our history

Foundation of the company



Going public

FSE: ADV



Going global

- Expansion in North America
- Revenue >USD 250 million



Scaling the business

- > 1800 employees
- Revenue > EUR 500 million
- Award-winning supply chain



1994 1999 2000 2006 2010 2013 2016 2020



First product

 Metro WDM for enterprise DCI



Adding Ethernet

 First fiber-based Ethernet services



Portfolio expansion

- Optical+Ethernet
- Network automation



Strategic acquisitions

- Synchronisation
- Software and virtualization

Open connectivity solutions for a connected world



ADVA worldwide

Our NUMBERS

- >EUR 500 million revenue¹
- ~1,800 employees²

Our CUSTOMERS

Hundreds of carriers Thousands of enterprises

Our LEADERSHIP

- #1 DCI³ enterprise
- #1 Ethernet access devices⁴
- #2 Network synchronization⁵



1) Annual 2017 – analyst consensus; 2) Sep 30, 2017; 3) Data Center Interconnect – Source: Ovum; 4) IHS 2016; 5) ADVA internal estimates

Network innovator – Speed for customers – Trusted partner



Our broad customer base









Global success with open connectivity solutions

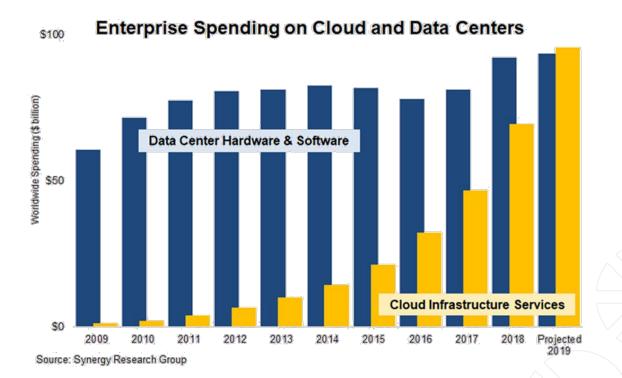




Data centers



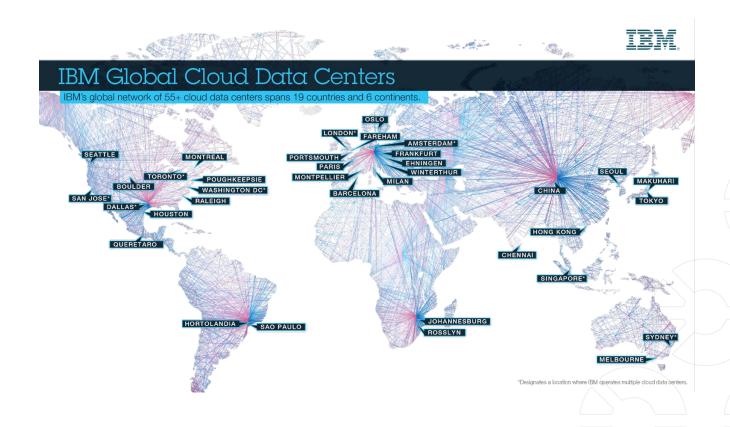
Data center CAPEX growth



Large market – even with low share



Data centers world wide



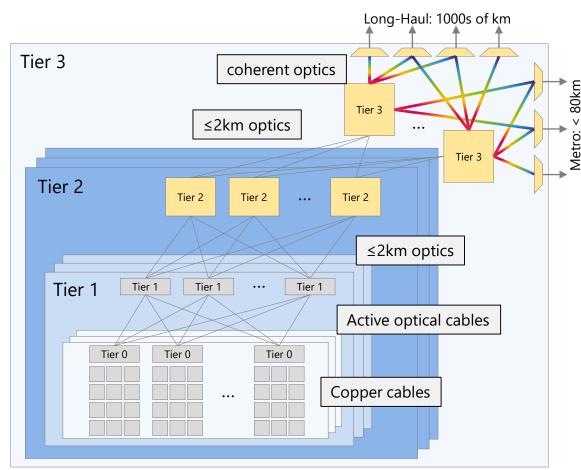


MS data center in Quincy, WA





Data center architecture



Tier 0 switches service a rack
Tier 1 switches service a "row"
(of racks)

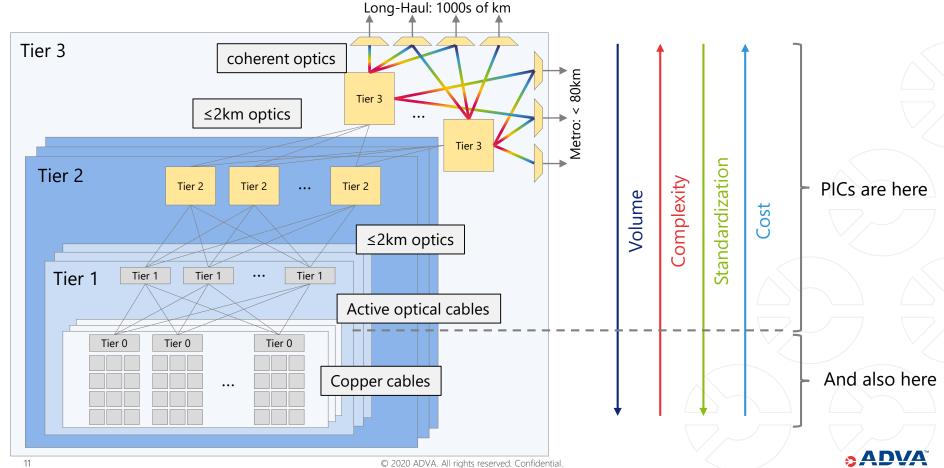
Tier 2 switches service a "Co-location"

Tier 3 switches service a datacenter

- Interface to long-haul network
- Also interface to metro network



Data center architecture





Photonic integrated circuits

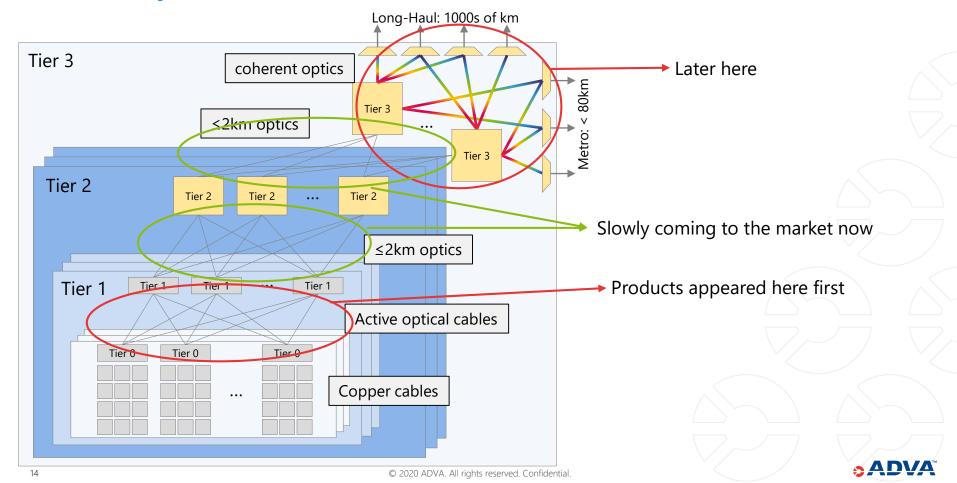


Flavors of PICs

	Silicon	InP	SiN	SiO	Polymer	LiNbO3
Waveguides	++	++	+++	+++	+	+
Fiber coupling	_	+	++	++	+++	+
Modulators	+	++			+++/	+++
Pol. converters	+++	+	-	-	-	-
Light sources		+++				
Photo detectors	++	+++	-	-	-	-
Footprint	+++	++	-	-		
Wafer size	+++		+	+	-	-
Yield	+++	+	++	++	+	-
Hybrid integration	++	-	+	+	+	
Packaging	++	-	+	+	+	-



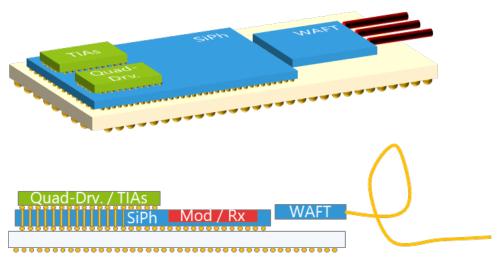
Silicon photonics in DCI



MASSTART

MASS manufacturing of TrAnsceiveRs for Terabit/s era





- Single optical alignment step for multiple I/Os
- Flip-chip assembly of driver and TIA on PIC
- Solder reflow compatible assembly

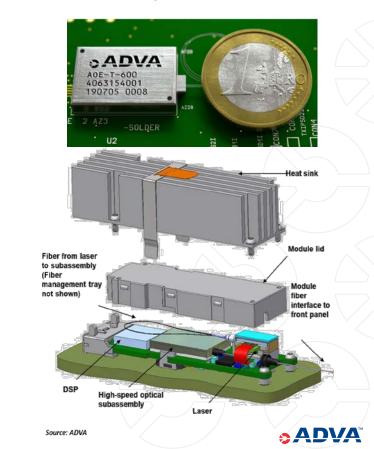
High-performance, low-cost assembly



IC-TROSA

Integrated Coherent Transmit Receive Optical Sub-Assembly

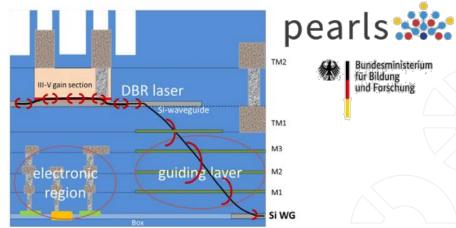
- Coherent optical engine for pluggables and line-cards
- Includes, modulator, receiver, driver, TIA and control electronics
- Solder reflow compatible
- BGA contacts for highest RF-performance
- 15 x 22.5 x 3.6mm (WxLxH) footprint
- OIF standard

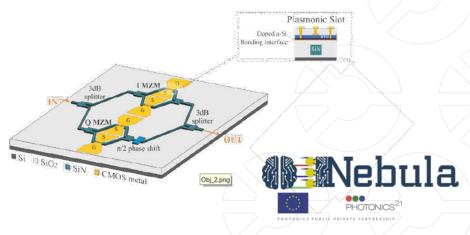


What's next for PICs?

- Integration of lasers on silicon?
- (Monolithic) integragtion of electronics?

New materials for higher speeds?







Conclusion

- DCI is a viable market (even with market low share)
- PICs can be a high-end market
- Packaging remains highest cost factor





Thank you

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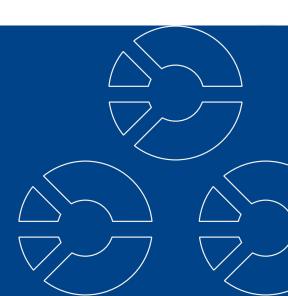


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Acknowledgement



Co-funded by the Horizon 2020 Framework Programme of the European Union

MASSTART project is co-funded by the Horizon 2020 Framework Programme of the European Union with Grant Agreement Nr.

825109. https://cordis.europa.eu/project/rcn/219912/factsheet/en

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