High-speed optical interconnects for intra- and inter-DC applications

Dr. Stelios PITRIS
Aristotle University of Thessaloniki (AUTH), Greece

online / October 5th – 8th / 2020
Photonics Days
Berlin Brandenburg
innovationconference

MASSTART

virtual conference session:
Data Center Interconnects – Towards Mass Manufacturing
online / October 6th 2020 / 4 – 7pm

High-speed optical interconnects for intra- and inter-DC applications

Stelios Pitris

Department of Informatics,
Center for Interdisciplinary Research & Innovation, Aristotle University of Thessaloniki (AUTH), Thessaloniki, Greece

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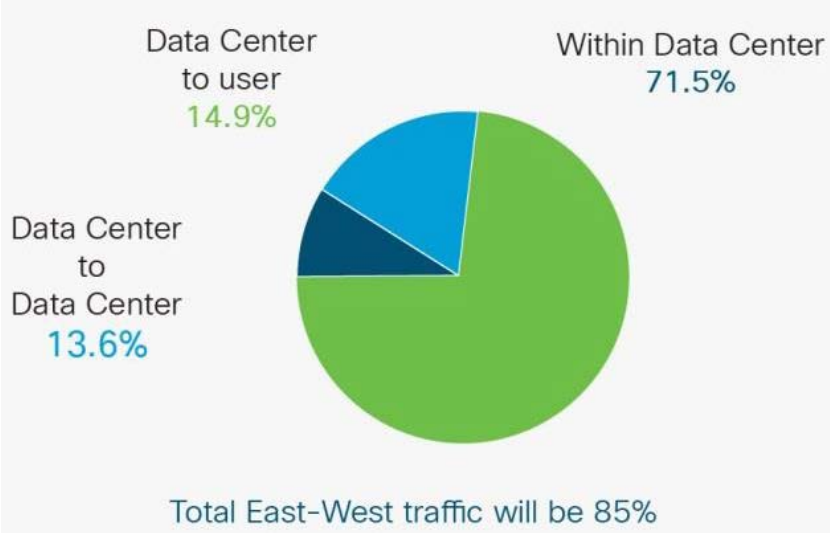
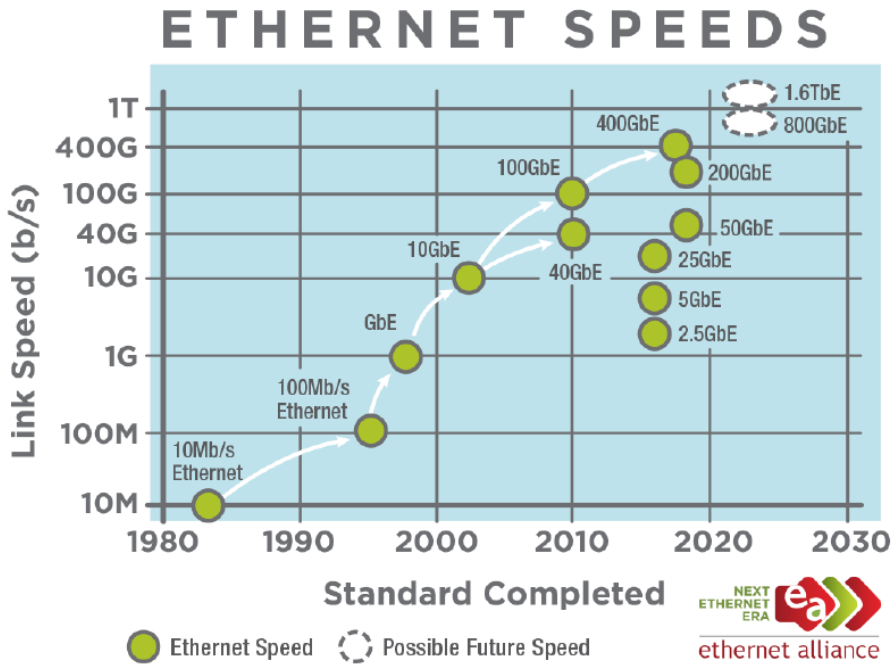
Motivation for high-speed Transceivers for DC operation

Global Data Center traffic by destination in 2021



Source: Cisco Global Cloud index, 2016-2021



Emerging DC Transceiver requirements

- ***High line-rate***
- ***WDM-functionality***
- ***CMOS-compatibility***
- ***Tight co-packaging with CMOS electronics***
- ***Ideally sub-V driving voltage***

Our work in DC transceivers & interconnect technology

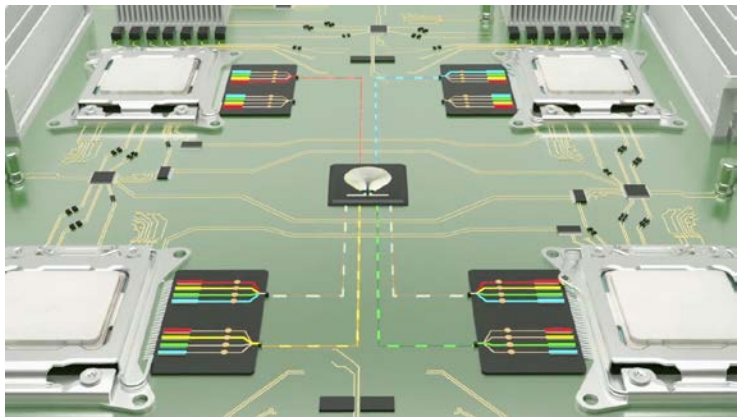
H2020-ICT-STREAMS
(Jan-2016-ended Nov 2019)

H2020-MASSTART
(January 2019-ongoing)

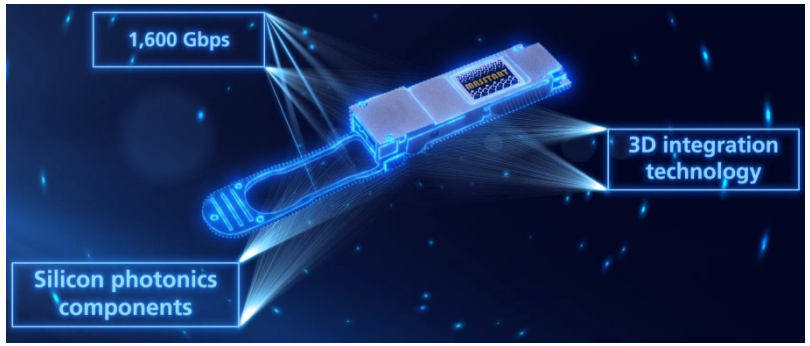
H2020-NEBULA
(Jan 2020-ongoing)

Target:

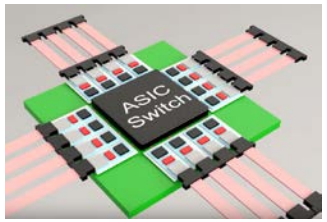
On-board interconnects for multi-socket computing

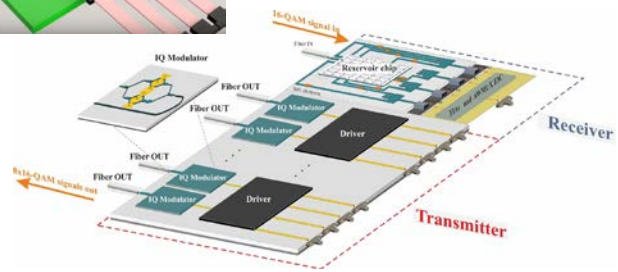


Mass-manufacturing of intra- & inter-DC transceivers



High-speed plasmonic transceivers for intra- & inter-DC

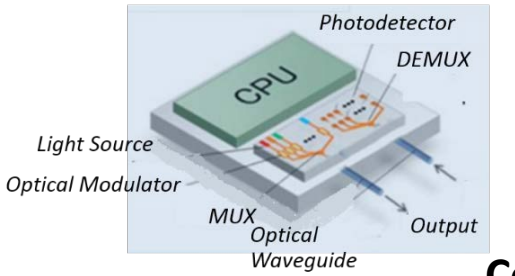




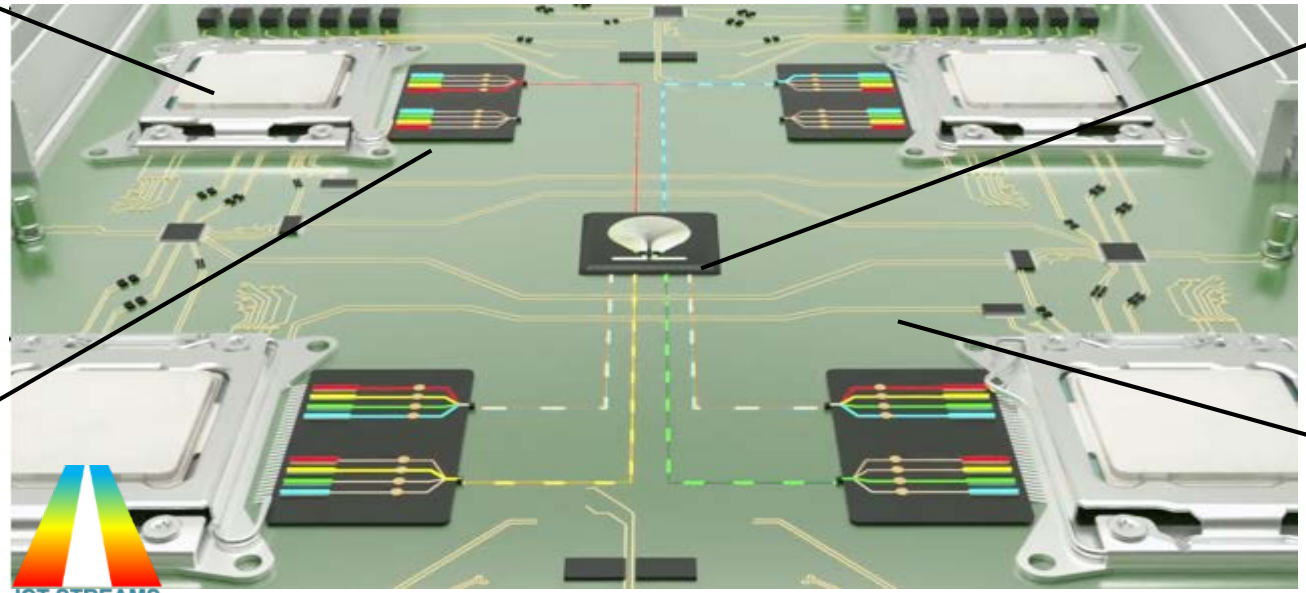
ICT-STREAMS: On-board interconnects for multi-socket boards

CPU socket

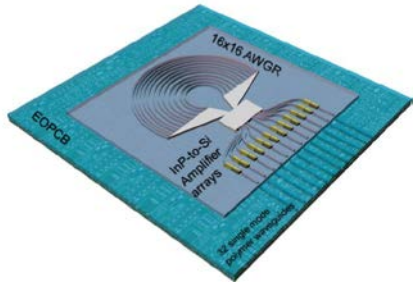
WDM Transceiver



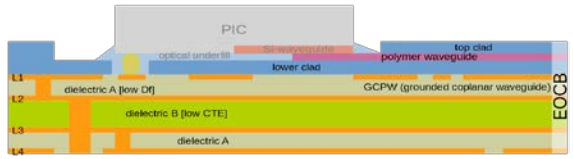
Envisioned Optical Multi-Socket Board in O-band



AWGR router



EO motherboard



ICT-STREAMS

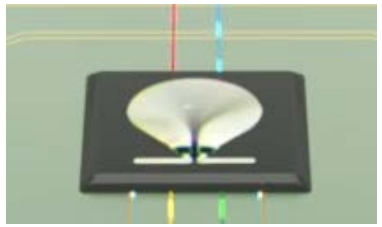
Coordinator: AUTH

Interconnection benefits

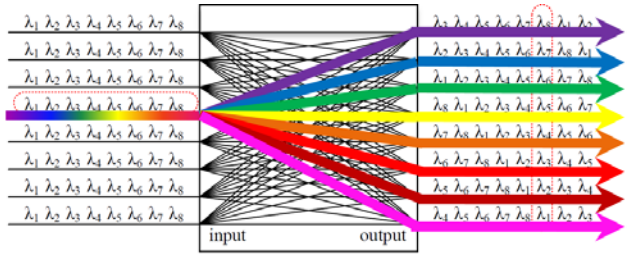
- ✓ *Strictly non-blocking all-to-all connectivity*
- ✓ *Suitable for multi-/broadcasting*
- ✓ *High number of ports (up to 32)*
- ✓ *High bandwidth optical links*
- ✓ *BW-independent low-latency links*
- ✓ *Passive λ-routing*
- ✓ *Relaxed assembly requirements (VS chip-scale)*
- ✓ *Low-loss interconnection via O-band polymer WGs*

Si-photonic cyclic passive router evolution within ICT-STREAMS

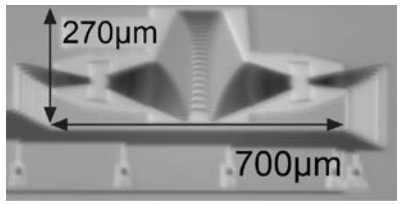
WDM Cyclic AWGR Router



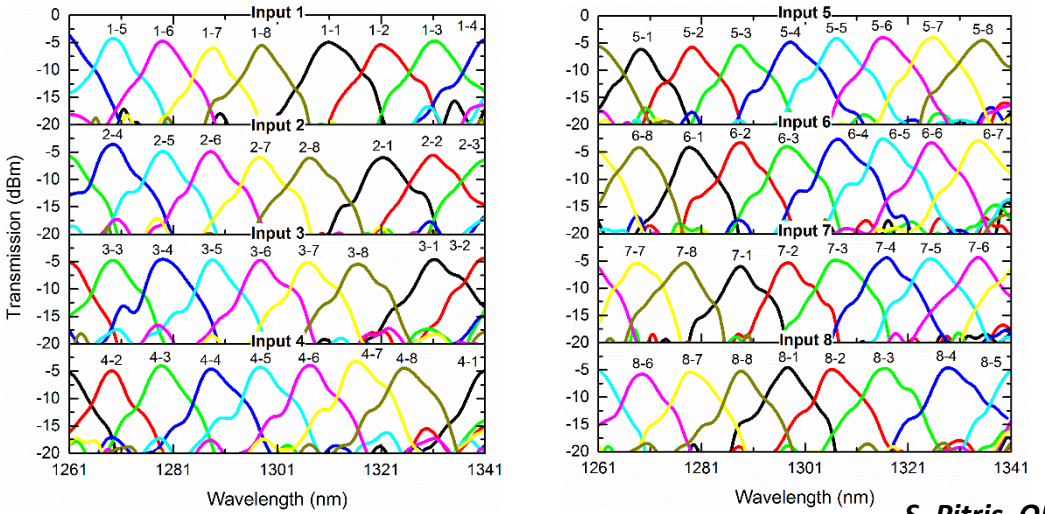
Cyclic-frequency all-passive wavelength routing



Si cyclic 8×8 O-band CWDM AWGR

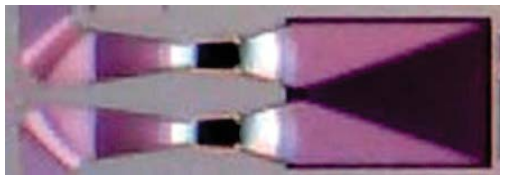


- ***10 nm (1.77 THz) channel spacing (1260, 1270,…, 1330 nm)***
- ***Cyclic operation validated***

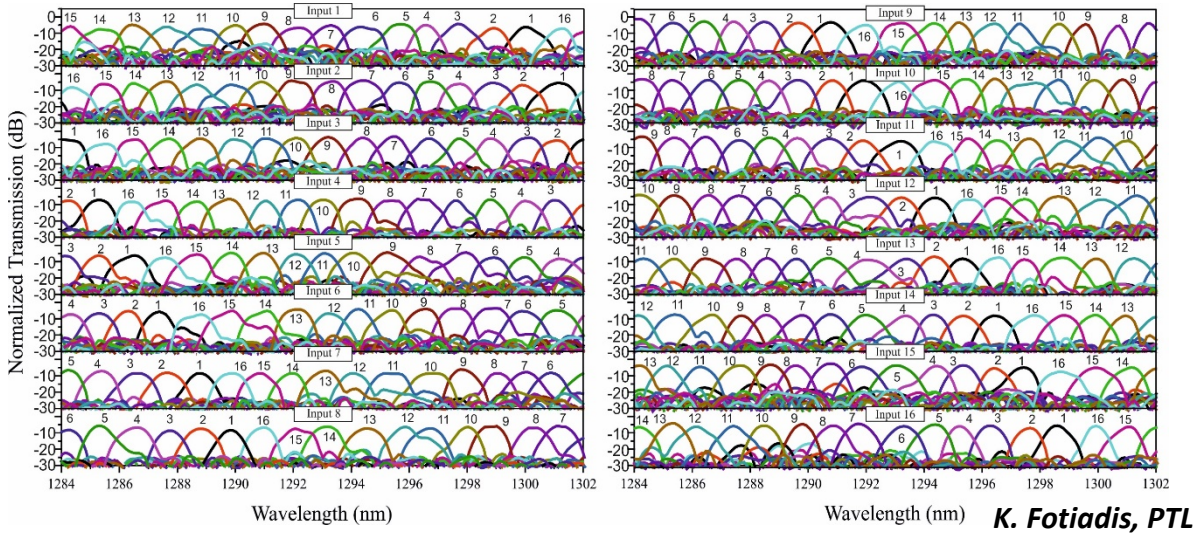


S. Pitris, OPEX 2018.

Si cyclic 16×16 O-band AWGR



- ***1.13 nm (200 GHz) channel spacing (1283,9,…, 1300,9 nm)***
- ***Cyclic operation validated***



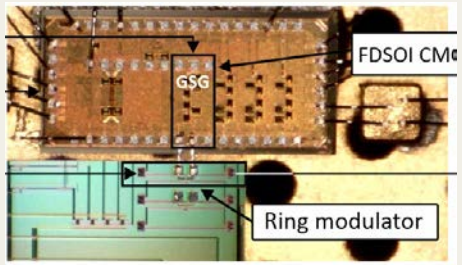
K. Fotiadis, PTL 2020

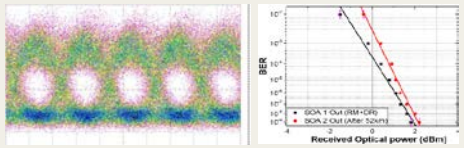
Si-photonic transceiver assembly evolution within ICT-STREAMS

From 50 Gb/s towards 800 Gb/s

50 Gb/s (1×50G)

MRM-based Tx with CMOS driver



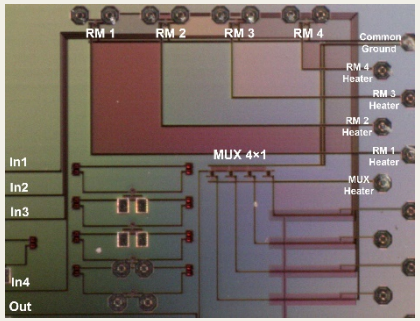


Highest O-band MRM BW×D (50Gb/s×52km)

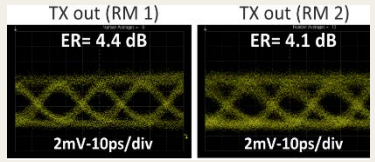
M. Moralis-Pegios et al., OECC/PSC 2019.

160 Gb/s (4×40G)

Silicon MRM-based Tx



Highlights

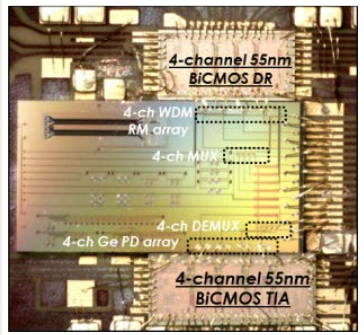


High-energy efficiency of 1 pJ/bit (incl heater)

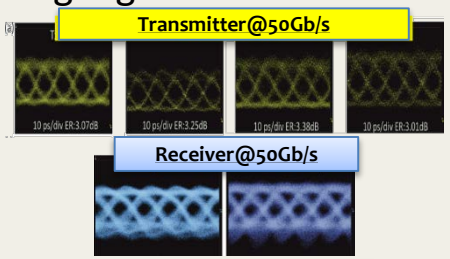
S. Pitris et al., OFC 2019.

200 Gb/s (4×50G)

Si TxRx with SiGe electronics



Highlights

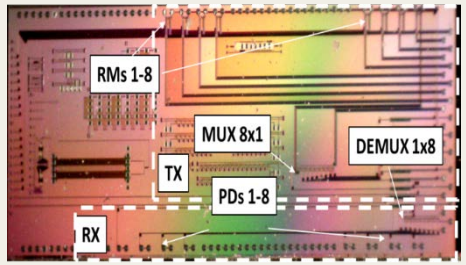


Total consumption 4.2 pJ/bit

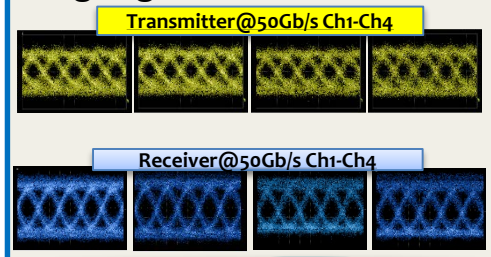
M.Moralis-Pegios et al., ECOC 2019.

400 Gb/s (8×50G)

Silicon MRM and Ge PD TxRx



Highlights

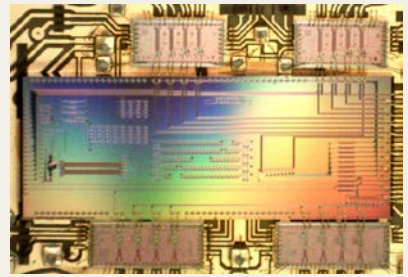


Record aggregated bandwidth for 50 Gb/s rate

To be submitted at OFC 2020.

400 Gb/s (8×50G)

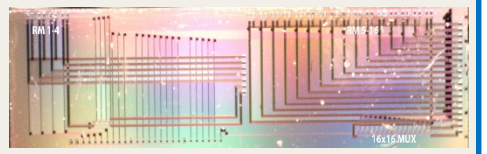
Assembled Si TxRx with SiGe electronics



Under evaluation

0.8 Tb/s (16×50G)

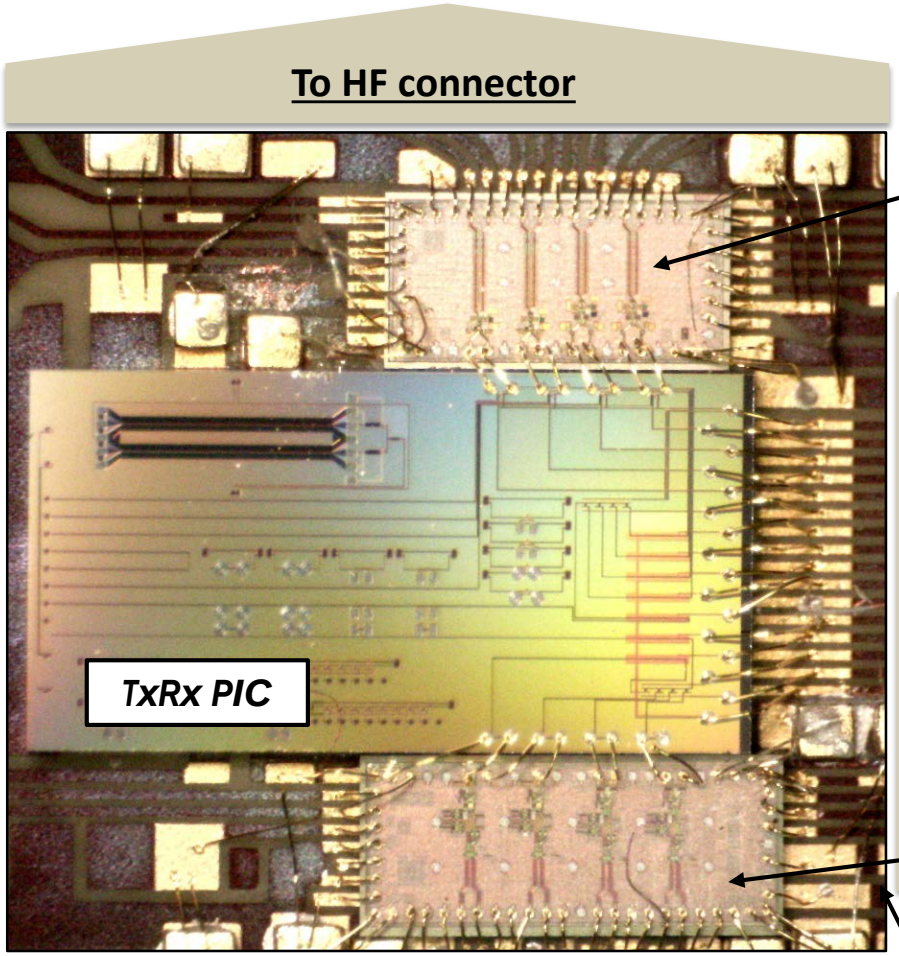
Silicon MRM-based Tx



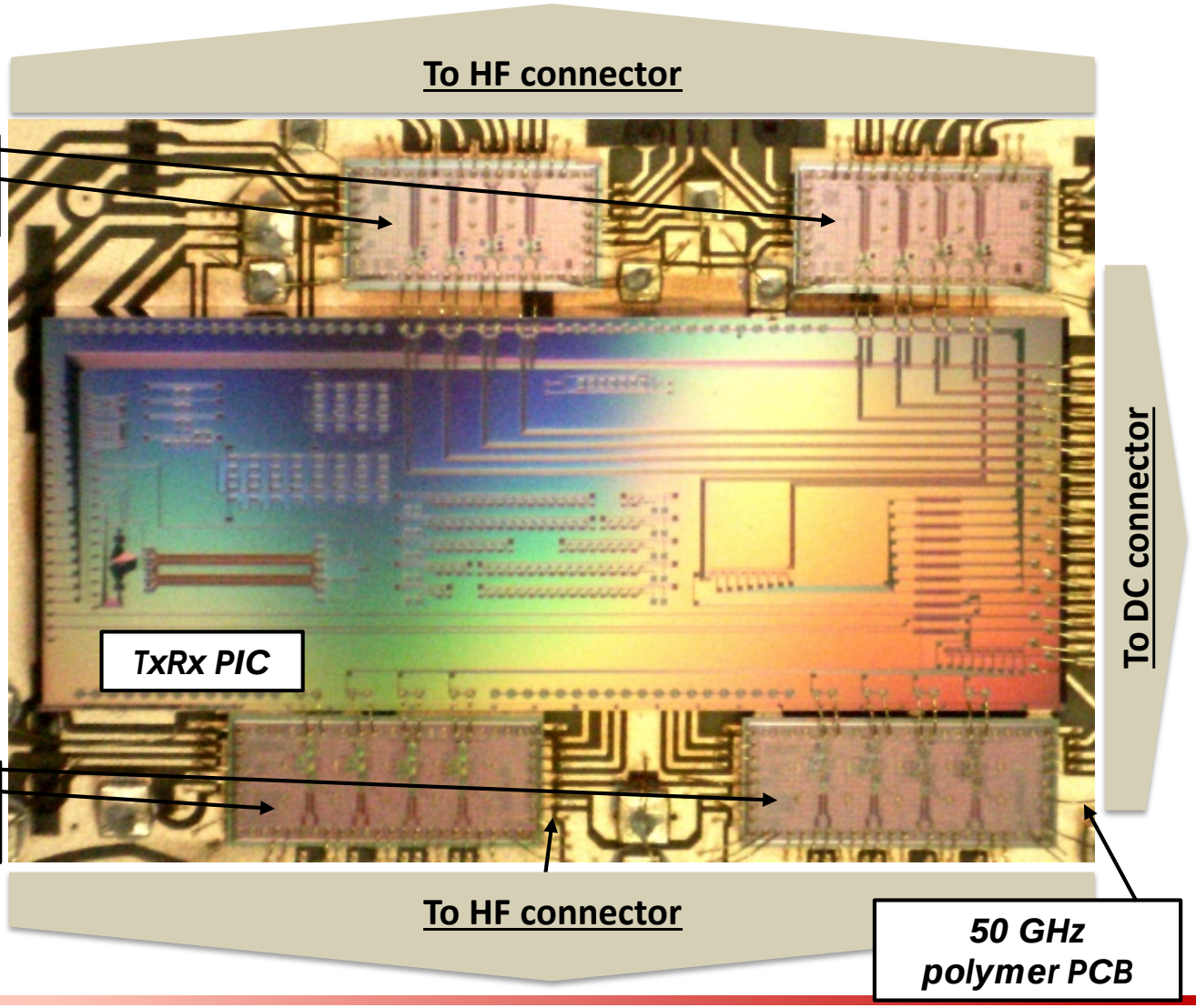
Under evaluation

Transceiver wire-bonded assemblies on PCB with 50 GHz DR/TIA electronics

WDM 4-channel TxRx assembly

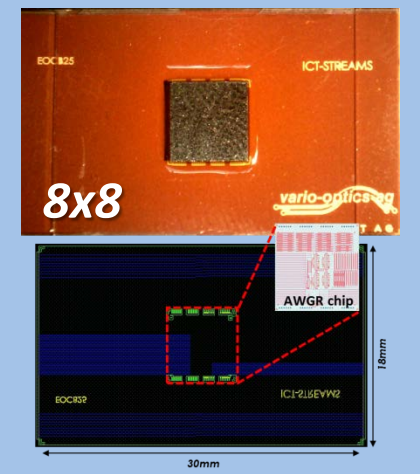


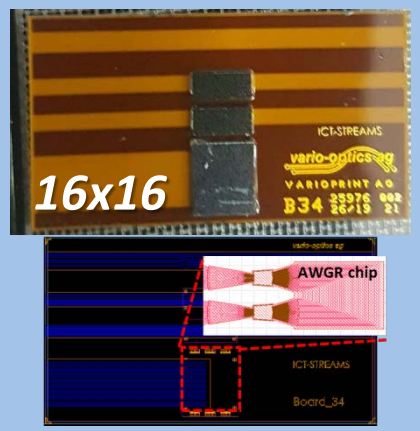
WDM 8-channel TxRx assembly



Currently under evaluation & further development

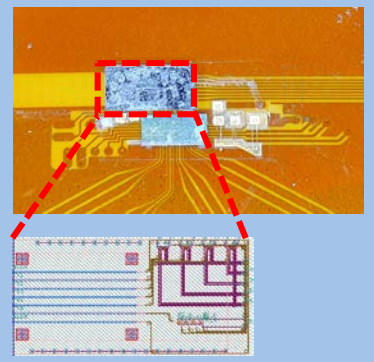
Board-pluggable Si-AWGR routers on polymer



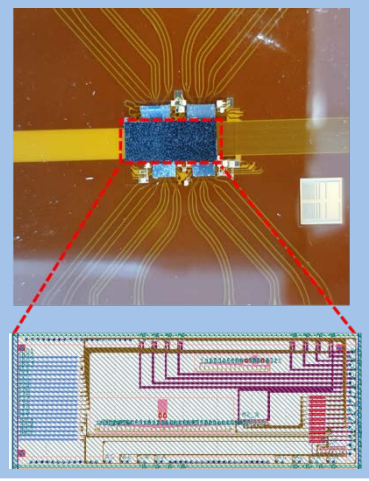


Board-pluggable TxRxs with EICs on polymer

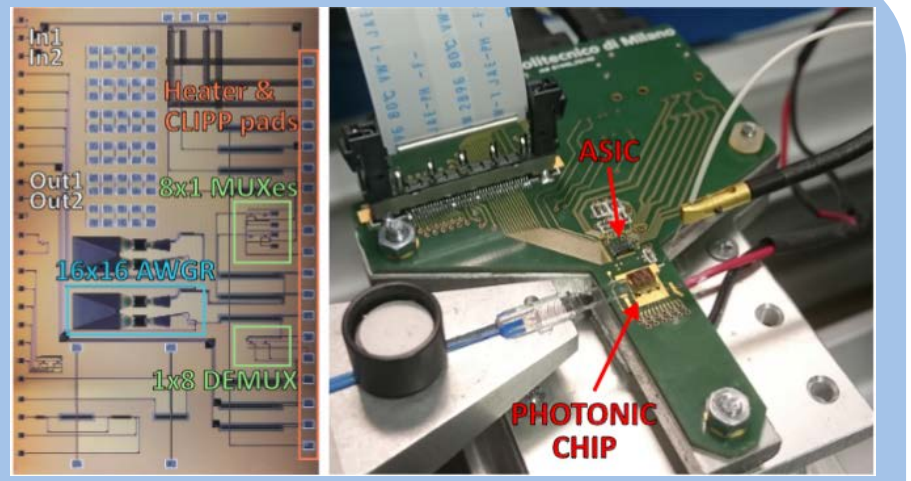
4x50G TxRx



8x50G TxRx



2-socket demonstrator with thermal drift compensation



F. Zanetto, JLT 2020.

Photonic chip

- *TxRx circuitry*
- *MUX circuitry*
- *Routing circuitry*

Feedback & control

- *Front-end ASIC*
- *FPGA control*
- *Hosting board*

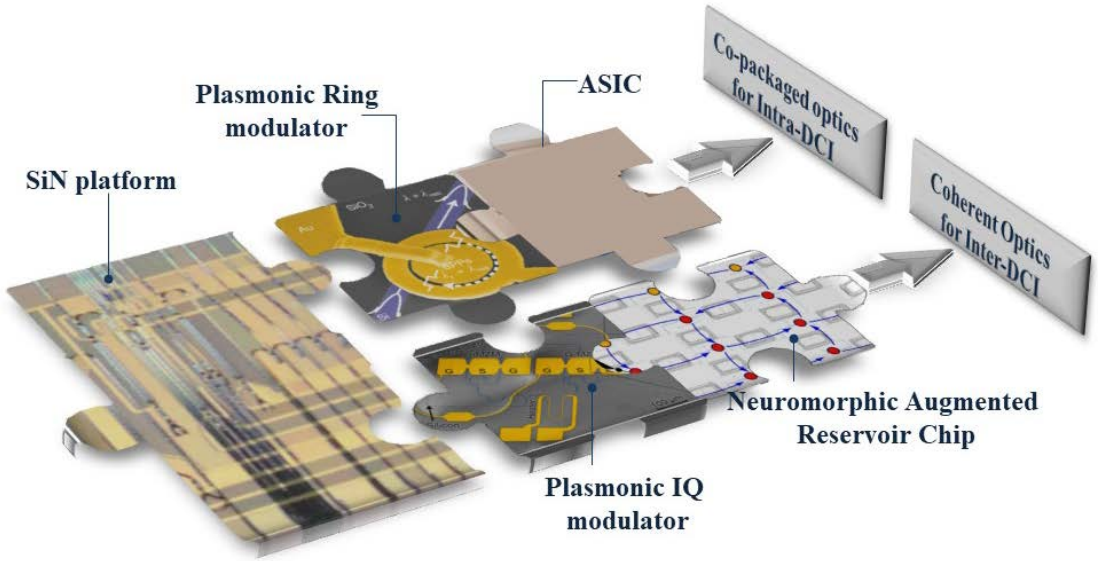
NEBULA: neuro-augmented TxRxs for intra- and inter-DC apps

NEBULA aims to deliver a powerful neuro-augmented 112Gbaud CMOS plasmonic transceiver platform for **Intra-** and **Inter-DCI** applications

Coordinator: AUTH

Key Technologies:

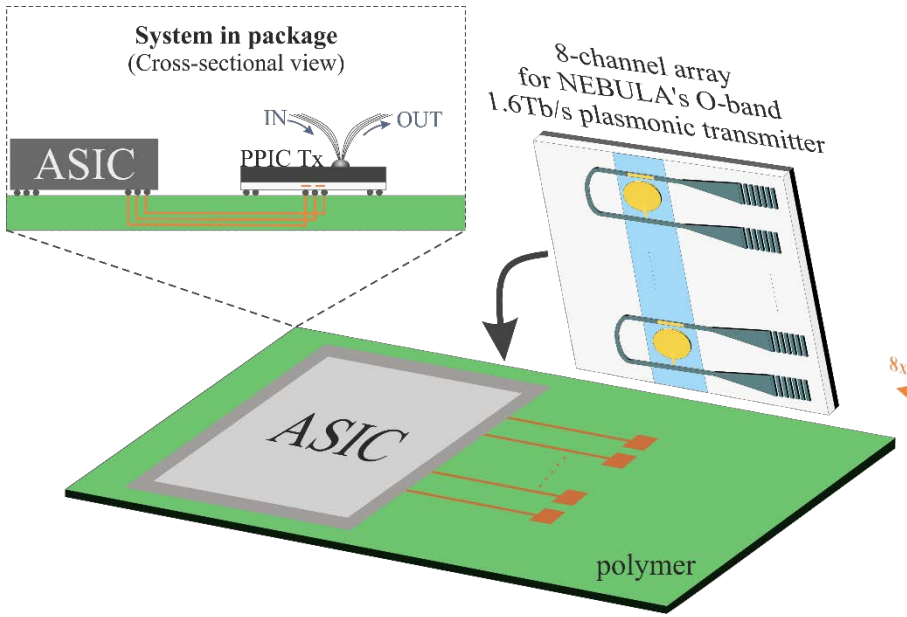
- 112GBaud plasmonic modulators on SiN based on ferroelectric BTO
- Loss-less thermal stabilization circuit
- Neuro-augmented all-optical DSP on the Rx
- 112GBaud BiCMOS ultra-fast electronics



NEBULA targeted transceiver prototype portfolio

Intra-DCI

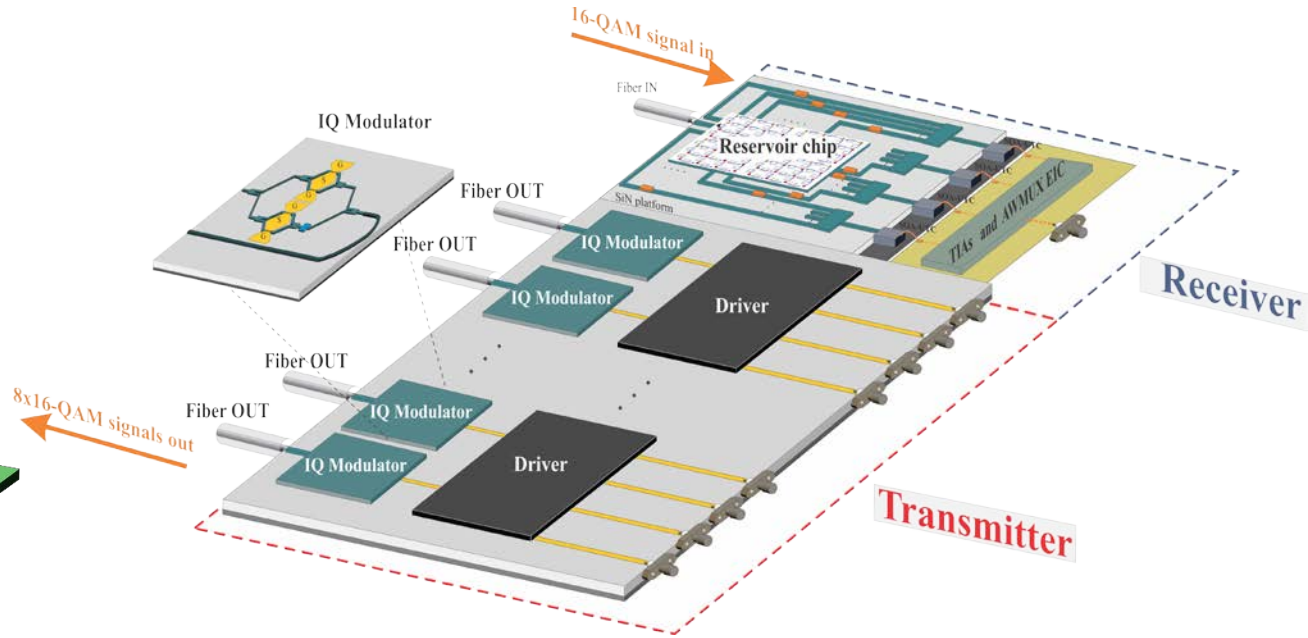
8-ch 112GBaud sub-volt O-band transmitter co-packaged with an ASIC



- ✓ Tx: 112Gbaud PAM4 disk/MZIR modulators
- ✓ Co-packaged with data generating ASIC

Inter-DCI

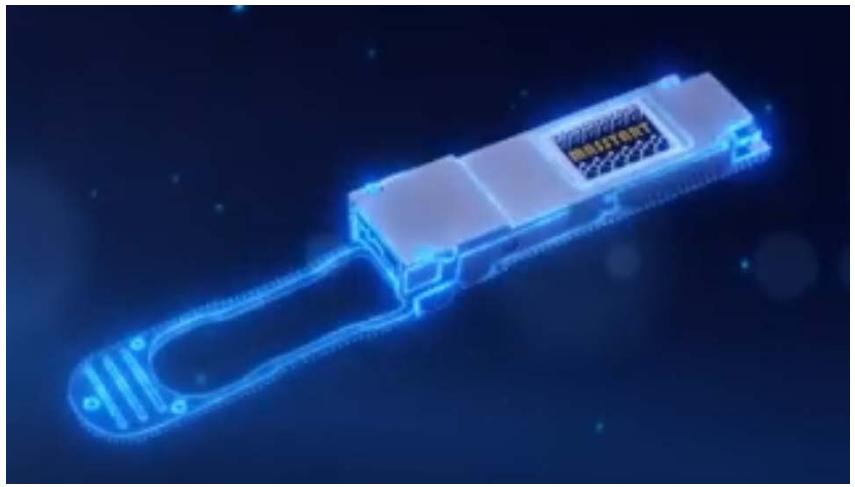
8-ch 112Gbaud 16-QAM C-band neuro-augmented transceiver prototype



- ✓ Tx: 112Gbaud PAM4 IQ modulators
- ✓ Rx: Reservoir-assisted DSP-free

MASSTART: mass manufacturing of intra- & inter-DC transceivers

MASSTART targets to deliver a pioneering assembly and characterization framework for high-speed photonic transceivers



Targeted transceiver prototypes:

- 4-channel PSM4 400G (56G PAM4) transceiver
- 8-channel WDM 800G (56G PAM4) transceiver
- 16-channel WDM 1.6T (56G PAM4) transceiver
- Coherent 600G 64QAM-DP transceiver

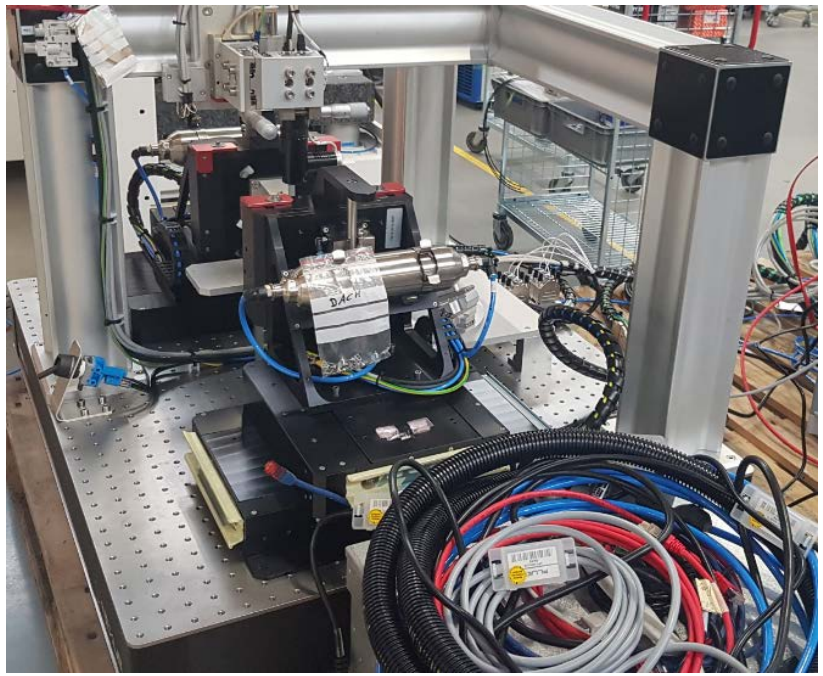
O-band for intra-DC

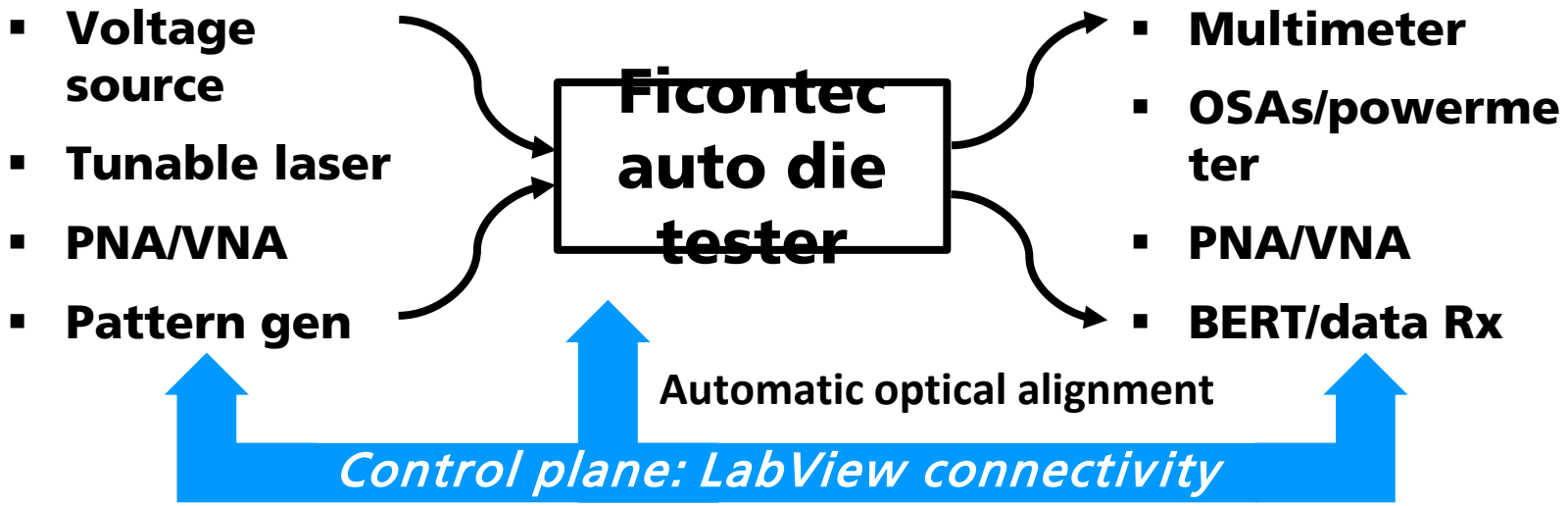
C-band for inter-DC

AUTH contribution: automated testing platform

Automated die tester probe setup by: ficontec photonics assembly & testing

Automation for various characterization tasks by: ARISTOTLE UNIVERSITY OF THESSALONIKI





Probe capabilities

- Dc probing
- RF probing
- Optical probing

Automated tasks

- Task #1: Passive characterization (frequency sweeping) & DC
- Task #2: Electrical characterization
- Task #3: E/O characterization
- Task #4: Data generation, transmission, reception & analysis

Work sum up

- **ICT-STREAMS: On-board interconnects for multi-socket server boards**
  - **Passive routing components**
  - **Transceiver PICs and assemblies: from 50G to 800G NRZ**
- **NEBULA: neuro-augmented TxRxs for intra- and inter-DC apps**
  - **Targeted intra-DC plasmonic transmitter co-packaged with ASIC**
  - **Targeted inter-DC plasmonic transceiver with neuro-augmented DSP-free reception**
- **MASSTART: mass manufacturing of intra- & inter-DC transceivers**
  - **Development of an automated die testing platform for high-speed transceiver components**

Thank you

Funding & AUTH teams

H2020-MASSTART (ongoing)

Dr. S. Pitris,
T. Chrysostomidis
Dr. A. Totovic
Dr. D. Tsiokos
Profs. K. Vyrsokinos & N. Pleros

H2020-NEBULA (ongoing)

Dr. S. Pitris
G. Mourgias
T. Chrysostomidis
G. Roumbos
D. Chatzitheocharis
N. Terzenidis, E. Chatzianagnostou
Profs. K. Vyrsokinos & N. Pleros

H2020-ICT-STREAMS (ended Nov 2019)

Dr. T. Alexoudi
Dr. S. Pitris
Dr. M. Moralis Pegios
Dr. G. T. Kanellos
Profs. K. Vyrsokinos & N. Pleros

OUR TEAM

WinPhoS Research Group http://winphos.web.auth.gr

SCHOOL OF INFORMATICS

SCHOOL OF ELECTRICAL & COMPUTER ENGINEERING

Aristotle University of Thessaloniki
SCHOOL OF PHYSICS

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MASSTART project is an initiative of the **Photonics Public Private Partnership** www.photonics21.org

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