

Advances in Silicon Photonics targeting next generation transceiver PICs

Stéphane BERNABÉ

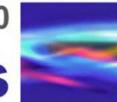
Project Leader – Photonic Circuits and Modules, CEA-Leti, France

online / October 5th – 8th / 2020

Photonics Days

Berlin Brandenburg

innovation conference

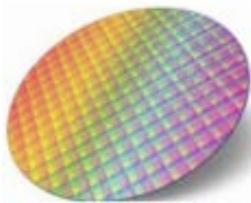


virtual conference session:

Data Center Interconnects – Towards Mass Manufacturing

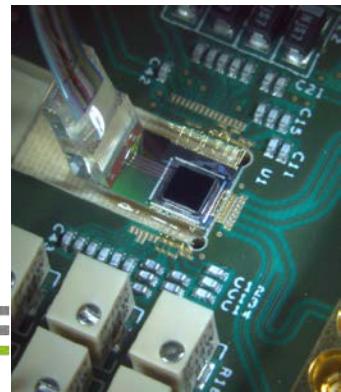
online / October 6th 2020 / 4 – 7pm

leti
cea tech



COSMIC €

CMOS Solutions for Mid-board Integrated transceivers with
breakthrough Connectivity & ultra low Cost (COSMIC)



ADVANCES IN SILICON PHOTONICS TARGETING NEXT GENERATION TRANSCEIVER PICS

Photonics Days Berlin Brandenburg | Stéphane Bernabé, Quentin Wilmart, Bertrand Szelag | 06.10.2020

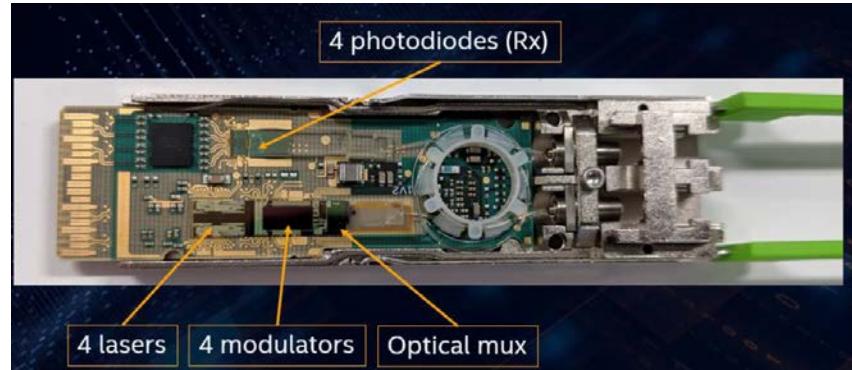
1 Today Status : SiPho platforms**2** New trends and requirements

- Ultra-low loss silicon waveguides
- 3D photonics : Si-SiN platform
- Laser integration
- Packaging

3 Conclusion

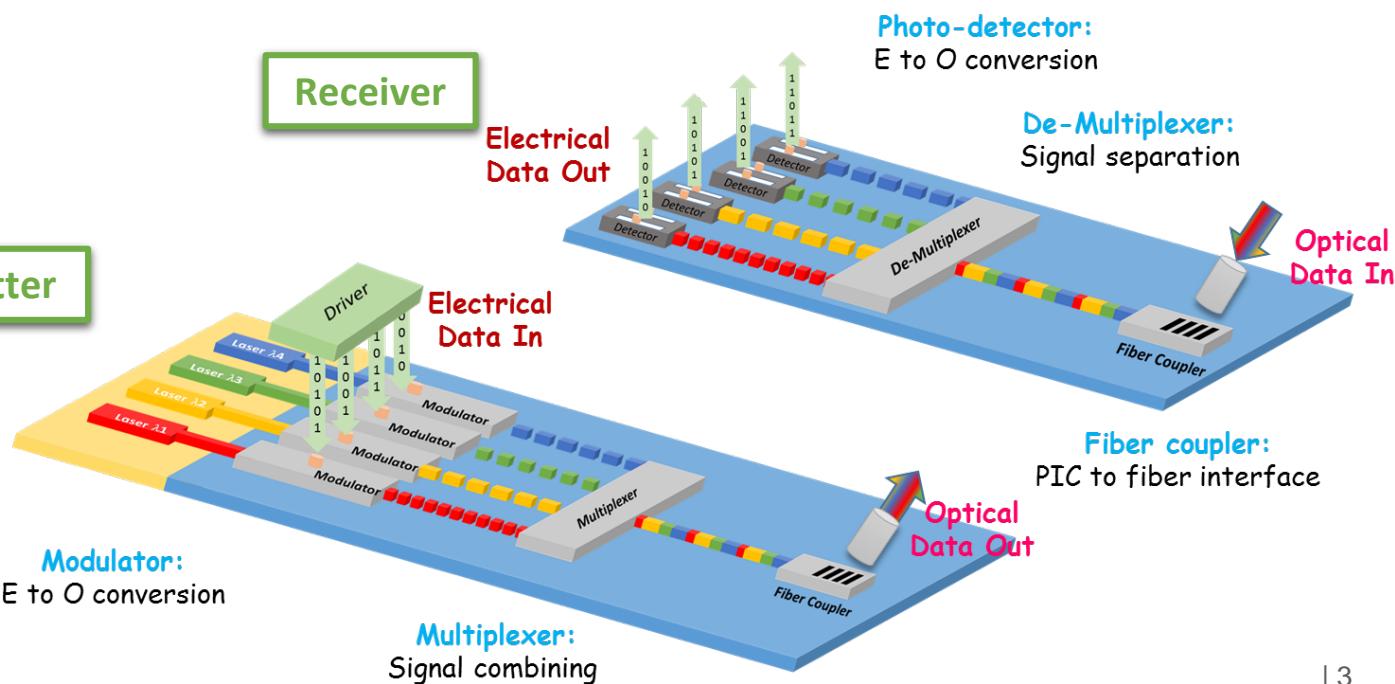
TODAY STATUS IN SILICON PHOTONIC TRANSCEIVERS

- Two big players
 - Intel (see pictures)
 - Cisco (Acacia/Luxtera/Lightwire)
- Start-ups
 - Ayar Labs
 - Rockley Photonics
- Commercial foundries
 - GlobalFoundries
 - TowerJazz
 - CompondTek
 - TSMC
 - IHP
 - AMF
- R&D Organizations & pilot lines
 - CEA-LETI, imec, VTT... (« RTOs »)
 - AIM



This image shows the optically connected FPGA board developed by Intel and Ayar Labs.
Source: Ayar Labs

Silicon Photonic Links

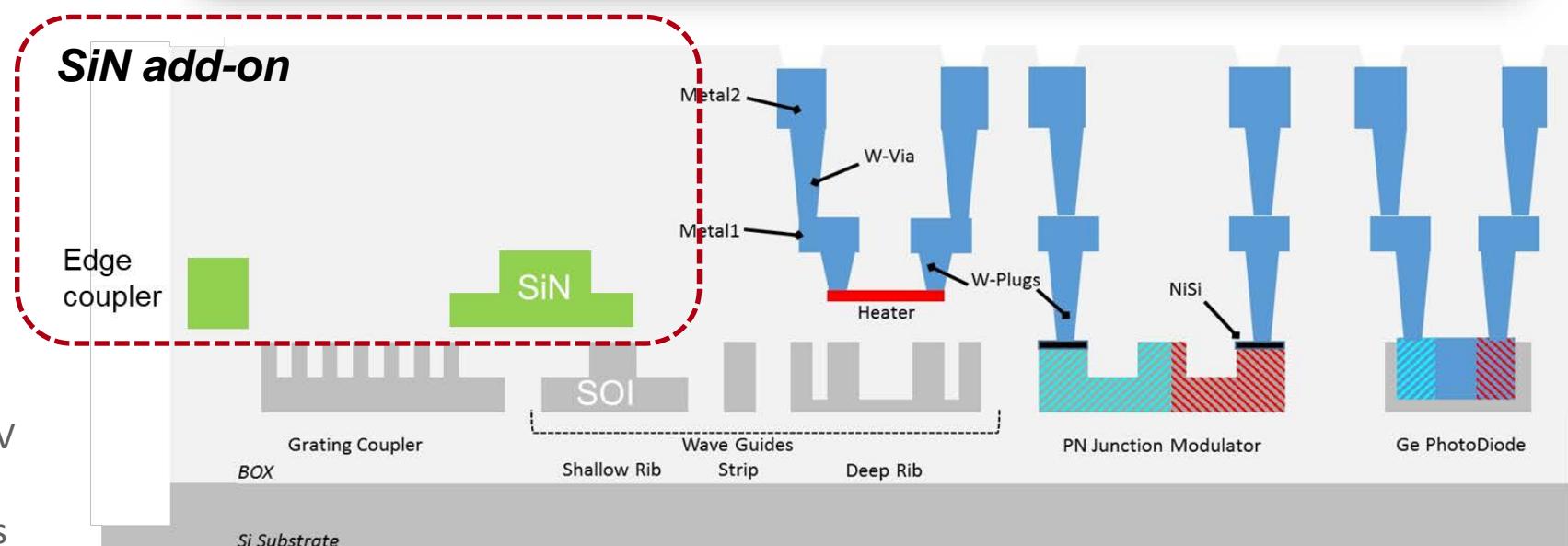


TECHNOLOGY KEY PROCESS FEATURES

- Si photonics platform
 - Substrates : SOI 310nm
 - > 200 steps
 - 24 litho levels
 - 40 metro/control steps
 - Flexibility: possibility to integrate the SiN layer for thermal properties or III-V epitaxies for hybrid lasers

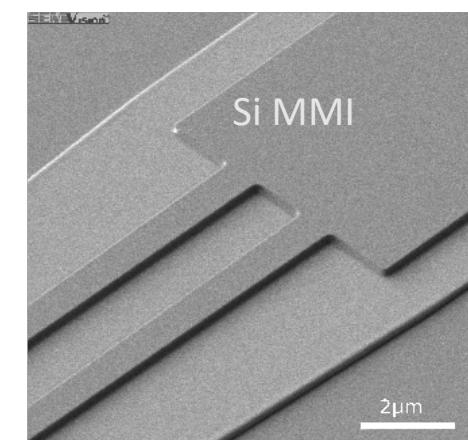
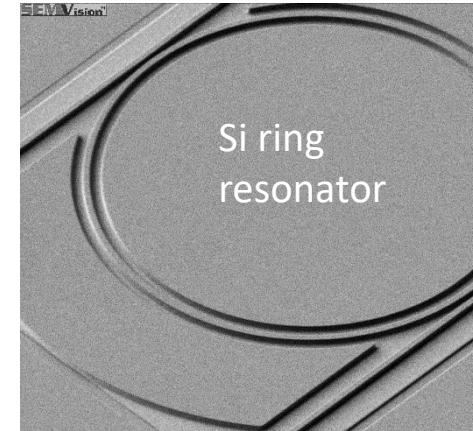
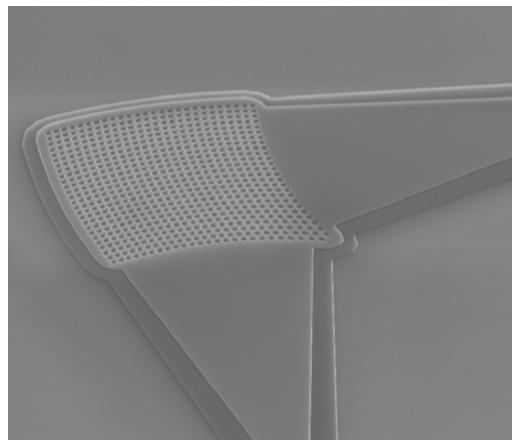
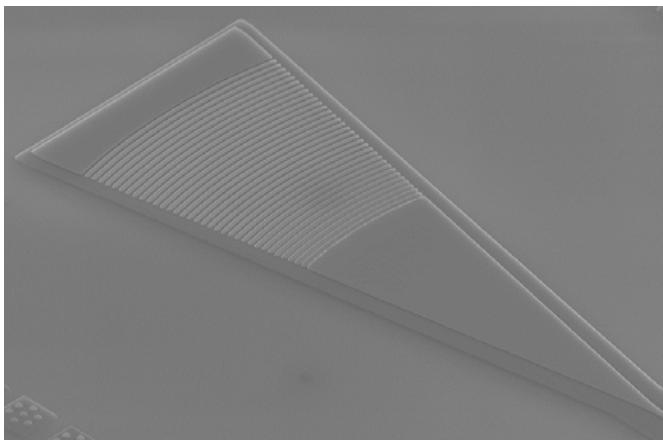
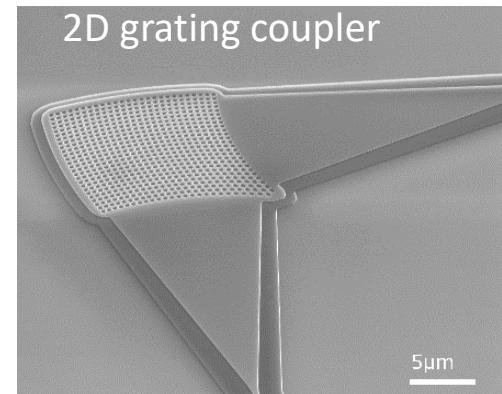
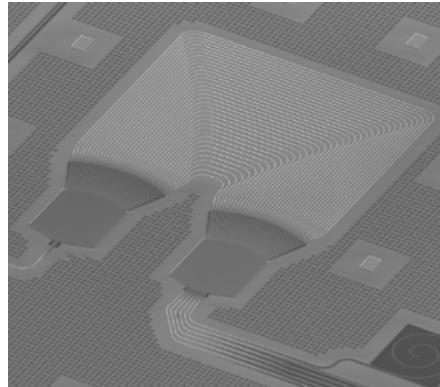


- Process building blocks
 - Multilevel silicon patterning
 - PN Silicon junctions
 - Germanium
 - SiN waveguides
 - Integrated resistance (heater)
 - Integrated laser (direct bonding of III-V wafers/dies)
 - Planarized BEOL : 2 AlCu routing levels



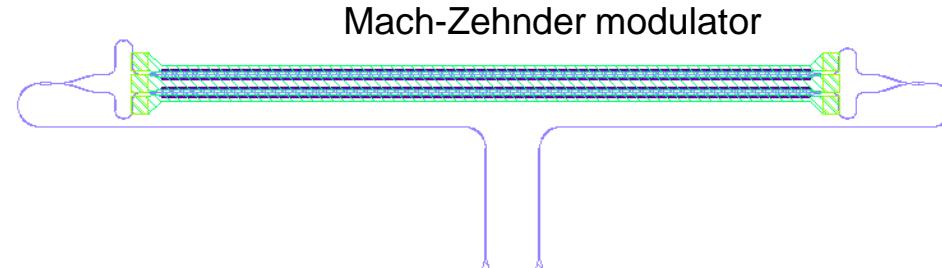
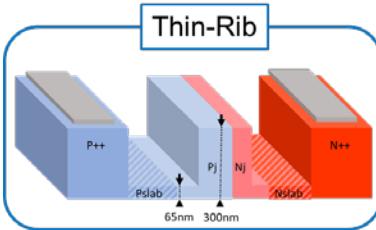
PASSIVE DEVICES

- Routing (waveguides, bends, crossings, splitters, MMI...)
- Wavelength Management
- Polarization Management
- Fiber Coupling
- DC phase shifter (with heater)



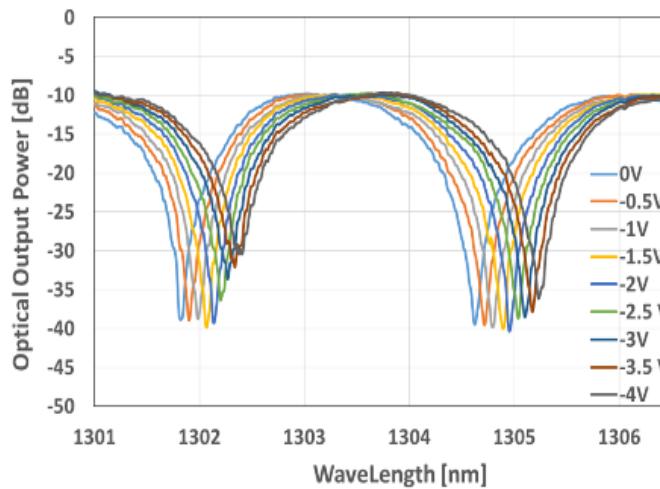
All these components available through Process Design Kits, as layout (p-cells) & models

ACTIVE DEVICES: P-N MODULATOR

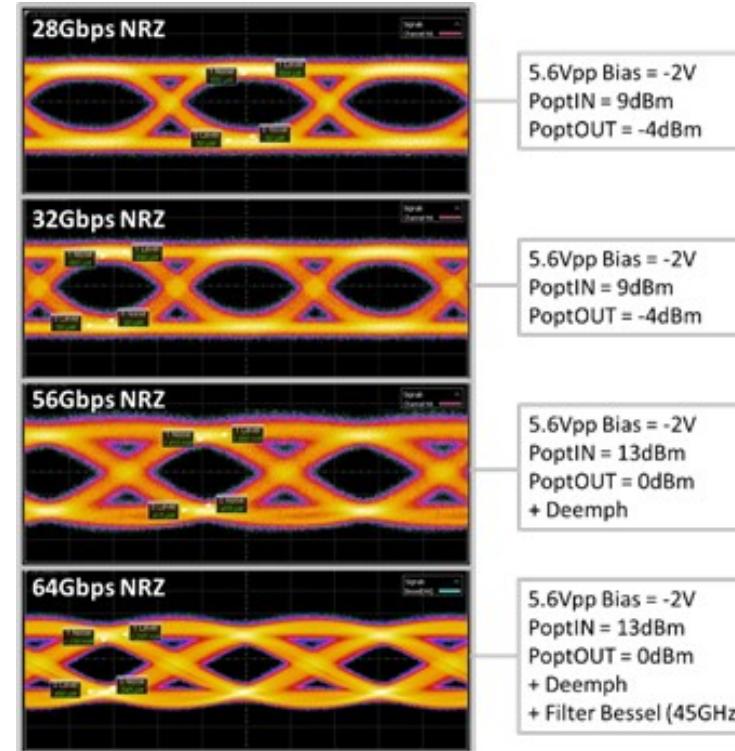


Electro-optical characteristics

Parameters	Thin-rib
V _{pILpi} @-2V (V.cm)	1,5
Losses (dB/mm)	0,7
BW@-6dB (GHz)	25

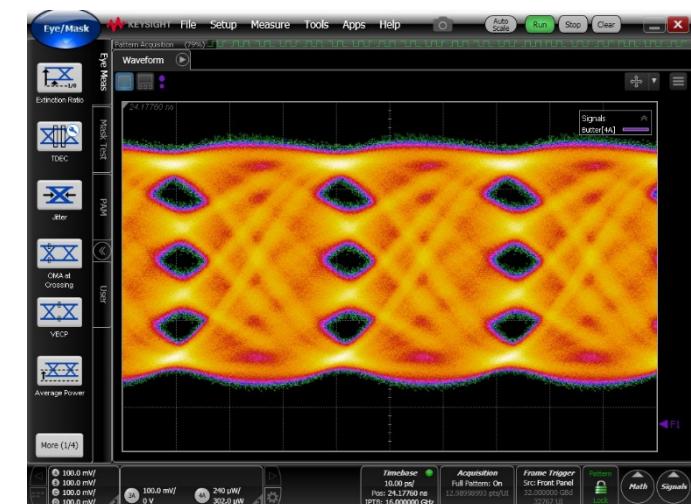


Modulation characteristics



32Gbaud PAM4

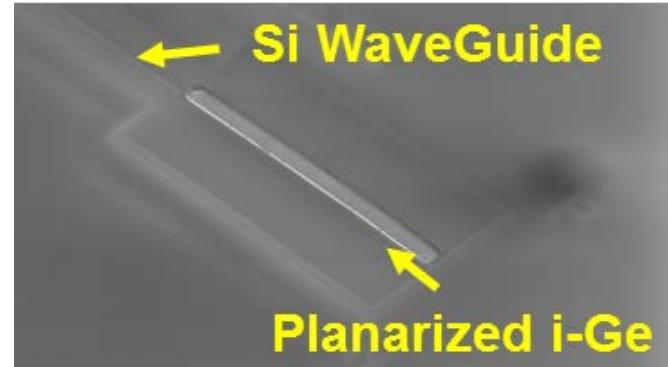
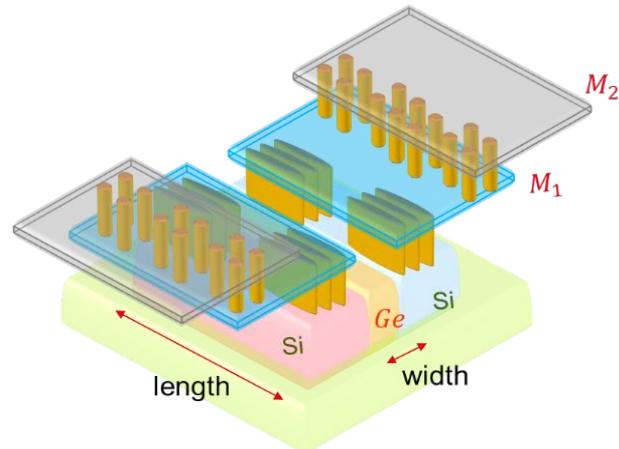
Bias PN : +4V
PDFA_IN = -10dBm
PDFA_OUT = 0dBm



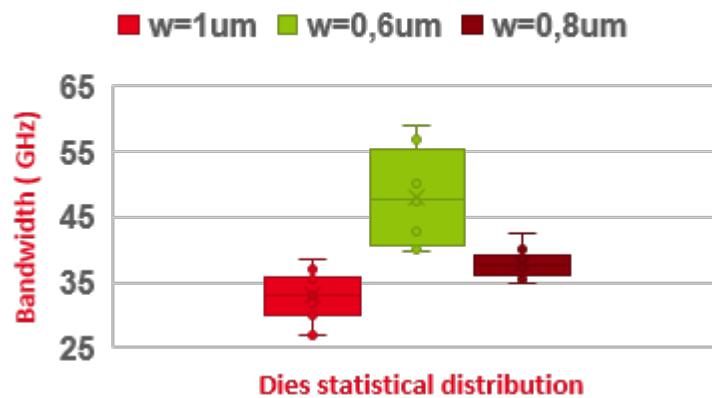
ACTIVE DEVICES: PHOTODIODE

High speed Si-Ge-Si photodiode

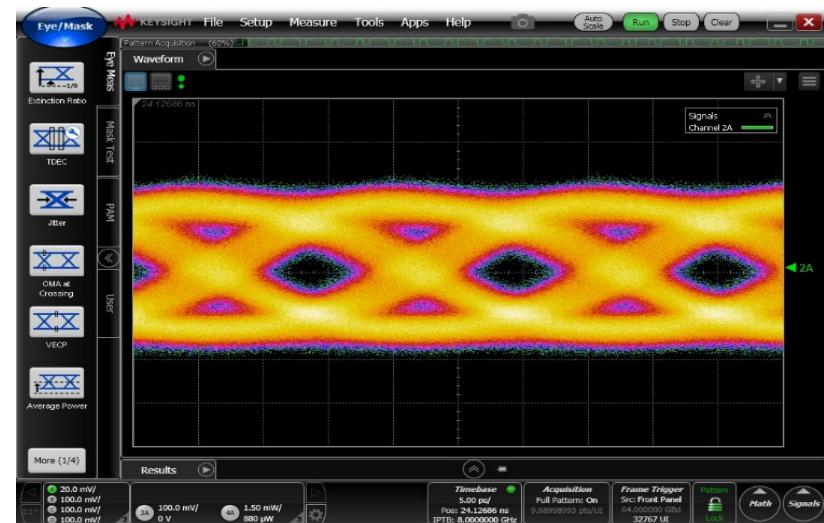
Width	0.8μm
Length	15μm
Responsivity	0.7 A/W
Dark current @ -2V	5 nA
BW @ -2V	> 35GHz



3dB bandwidth

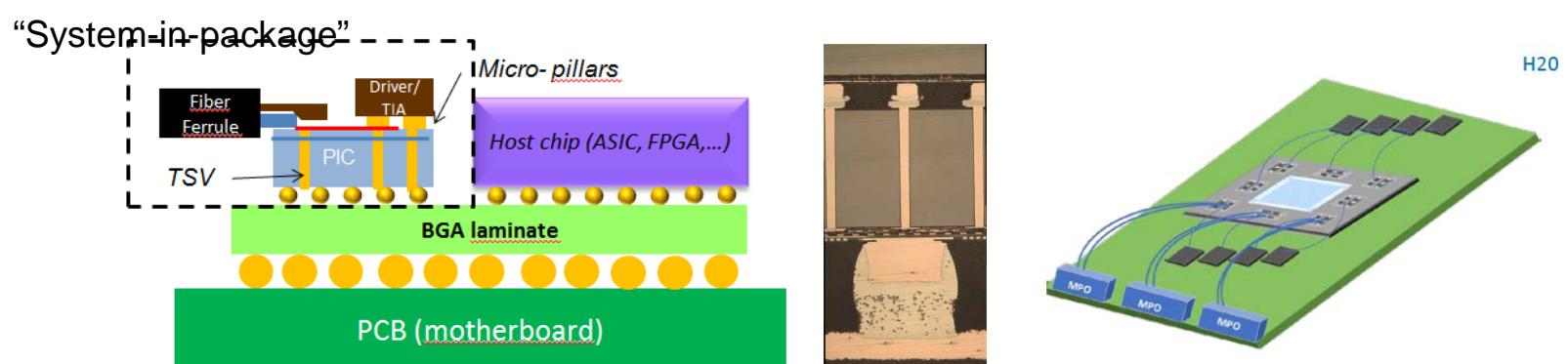
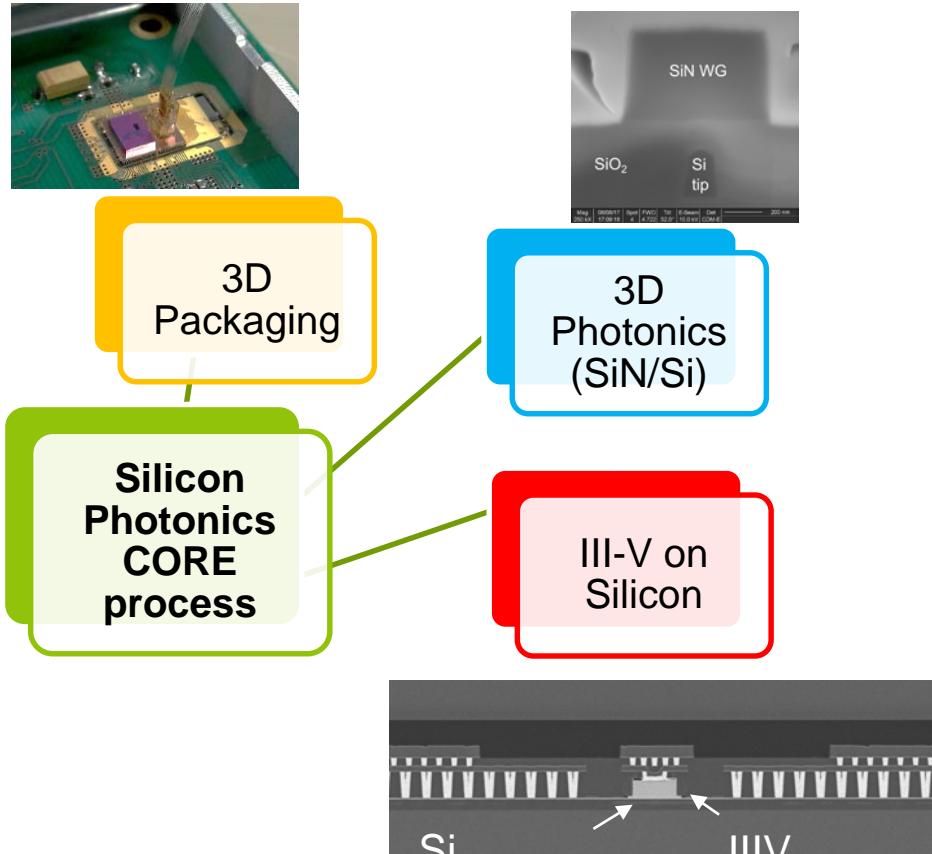


Eye diagram at
64Gbps NRZ:
BER=3 * 10⁻⁵
(SNR=4)

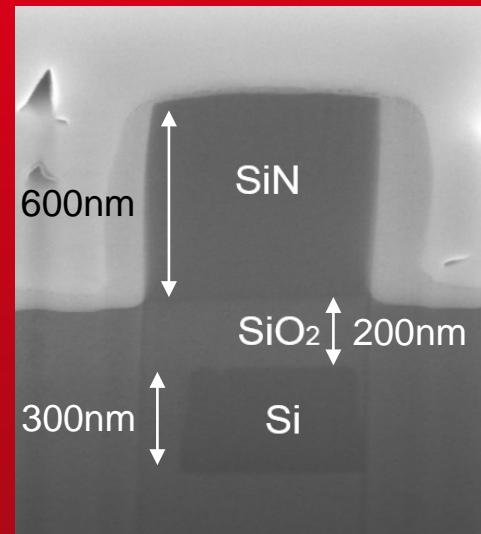


NEW TRENDS AND REQUIREMENTS

- **Increasing Data rate**
 - 800 Gbps and more
 - 25-50 GBd per channel
 - WDM, IQ modulation, PAM-4
- **Increasing density**
 - Tbps / mm²
 - Dense I/O connections
 - Co-packaging close to the host chip
- **Increasing Complexity**
 - Larger circuits
 - Increased number of I/Os
 - Complex routing
- **Laser source integration**



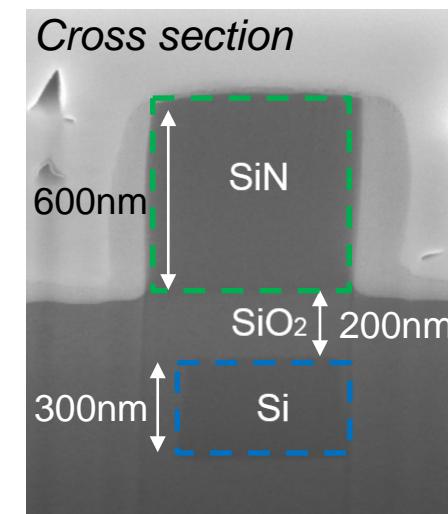
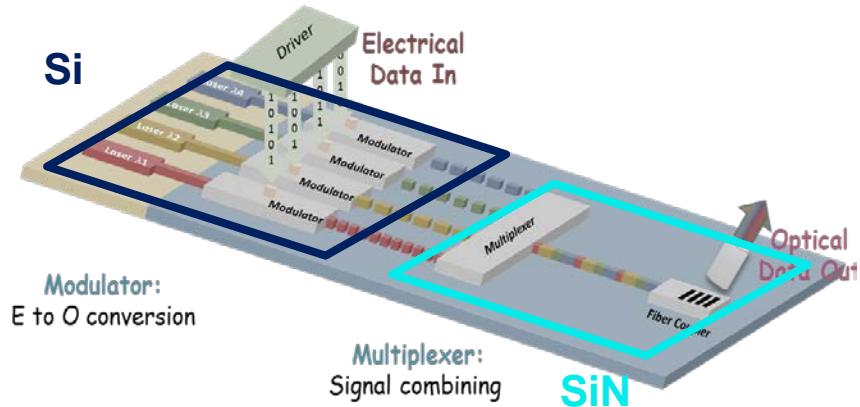
SILICON NITRIDE ADD-ON



ADD-ON: SILICON-NITRIDE AS A PHOTONIC LAYER

Why Silicon nitride:

- Low refractive index ($n_{\text{SiN}} = 1.88$)
→ less sensitive to fabrication imperfections
- Waveguide: 0.6dB/cm
- Low thermo-optic coefficient ($\sim 2 \times 10^{-5} \text{ K}^{-1}$)
→ Temperature quasi-insensitive **multiplexer**
- Broadband coupling scheme

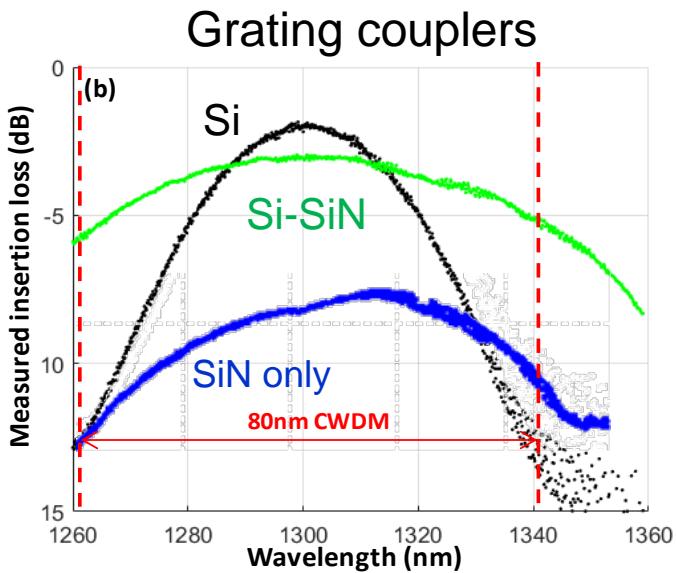
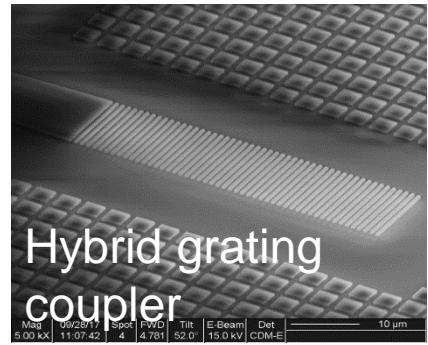


SiN BROADBAND FIBER COUPLERS

SiN-Si hybrid grating coupler

- 2-layers grating SiN-Si
- 2.8 dB insertion loss
- -1dB BW ~ 50nm

→ CWDM components wafer level testing
(broadband)

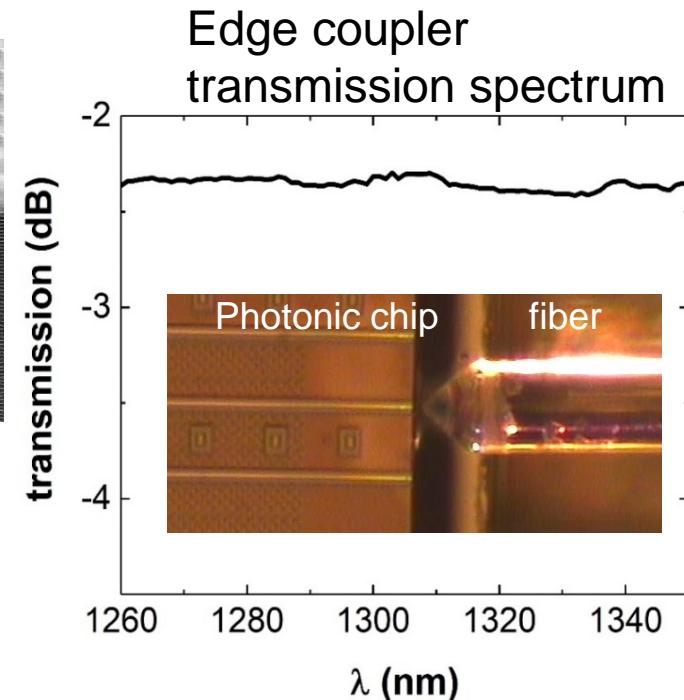
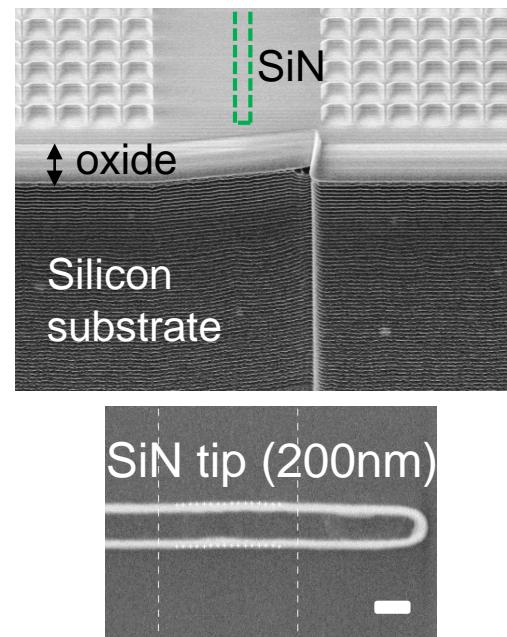


Hybrid grating coupler

Q. Wilmart et al., Appl. Sci. (2019)

Edge coupler with SiN taper

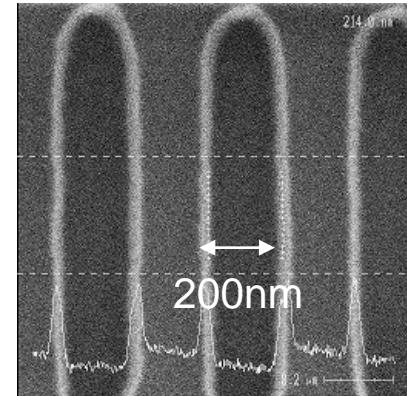
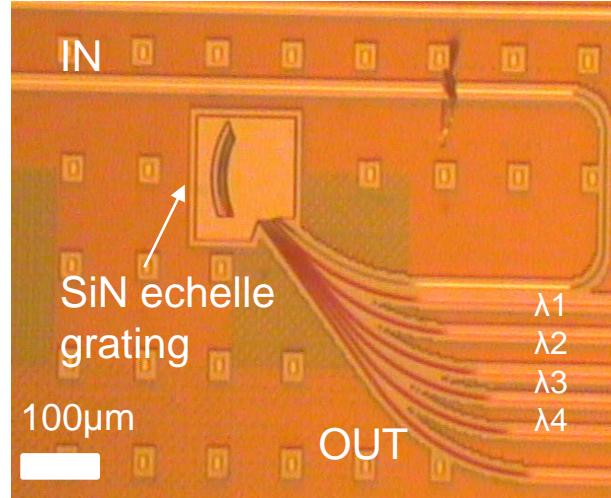
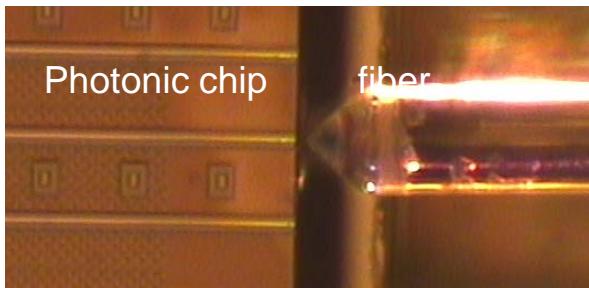
- Lensed fiber : MFD = 2.5μm
- SiN inverse taper
- Deep trench by dry etching
- Coupler insertion loss : < 2.4dB (O-band)
- For CWDM modules



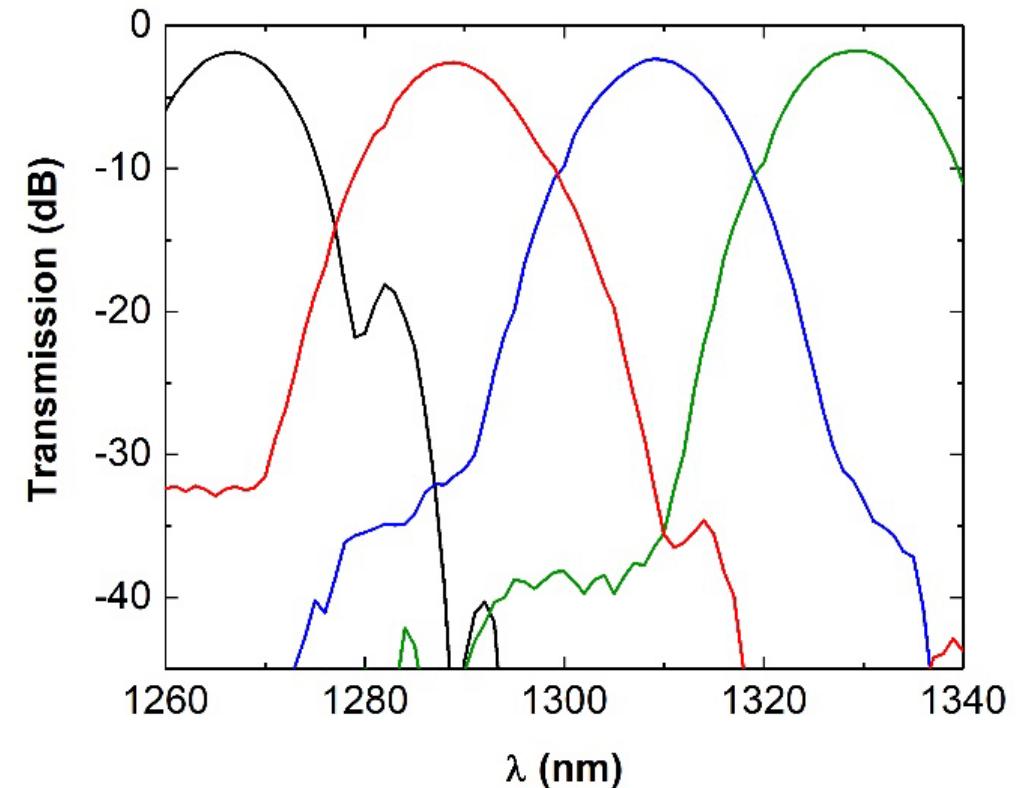
SiN CWDM MULTIPLEXER

SiN Echelle grating MUX

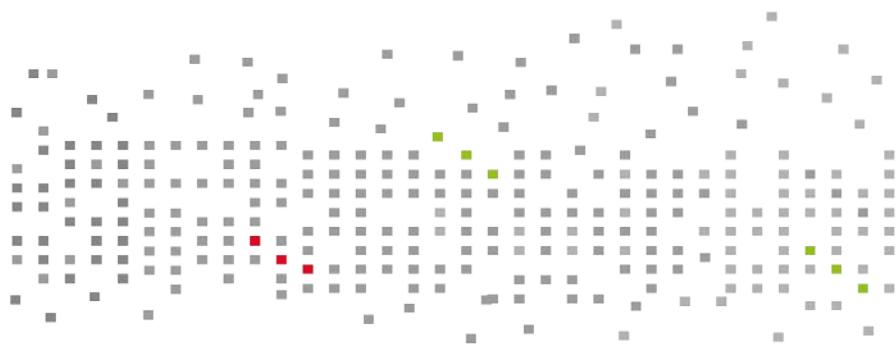
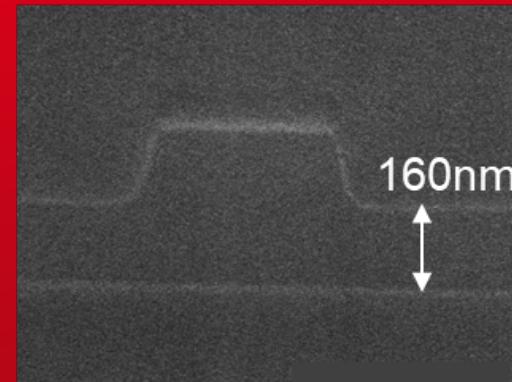
- 4 channels CWDM (O-band)
- Edge coupling measurement
- 193nm DUV photolithography of the SiN bragg grating
- Insertion loss : < 2.5dB
- Crosstalk < -30dB
- -1dB bandwidth ~8nm
- Thermal sensitivity: 13pm/K



SiN Bragg grating



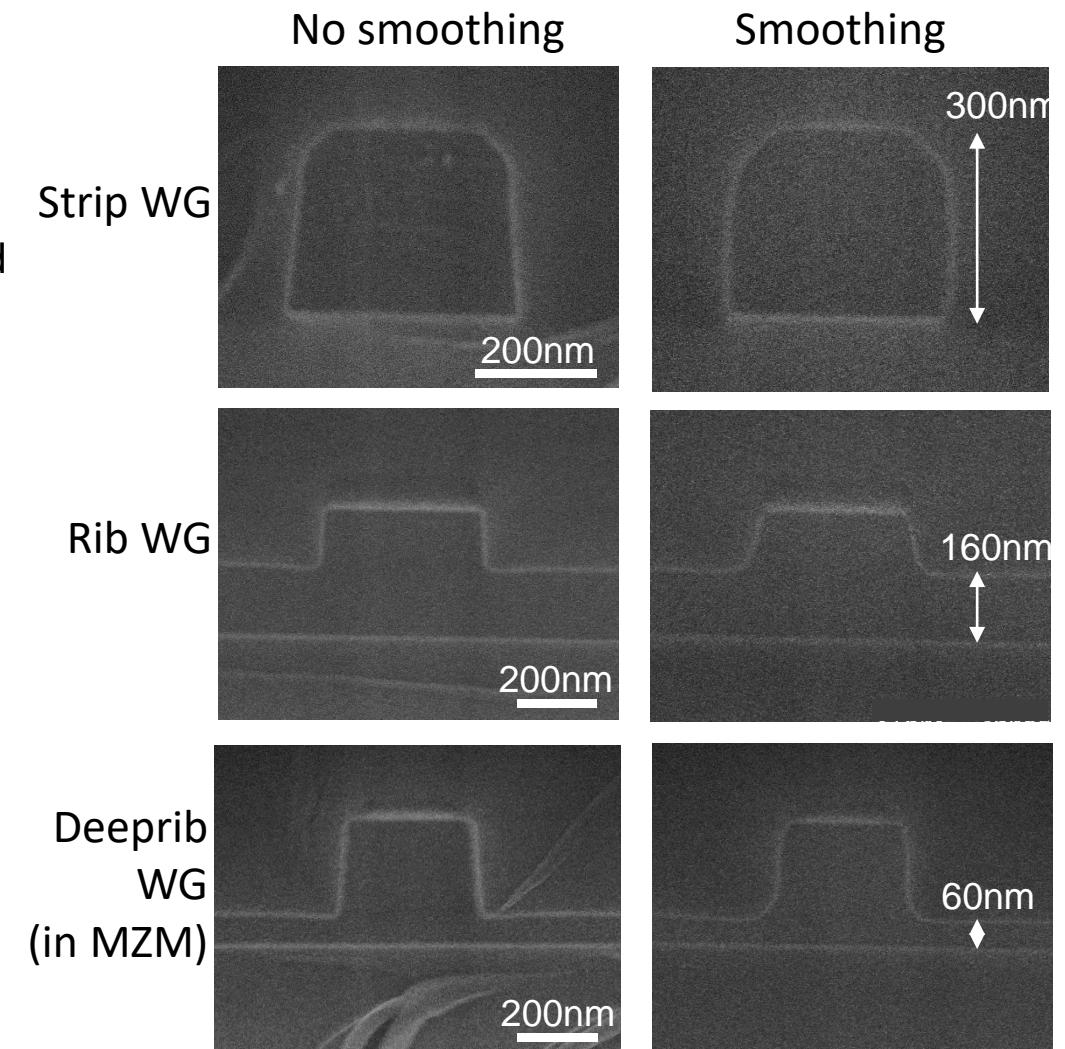
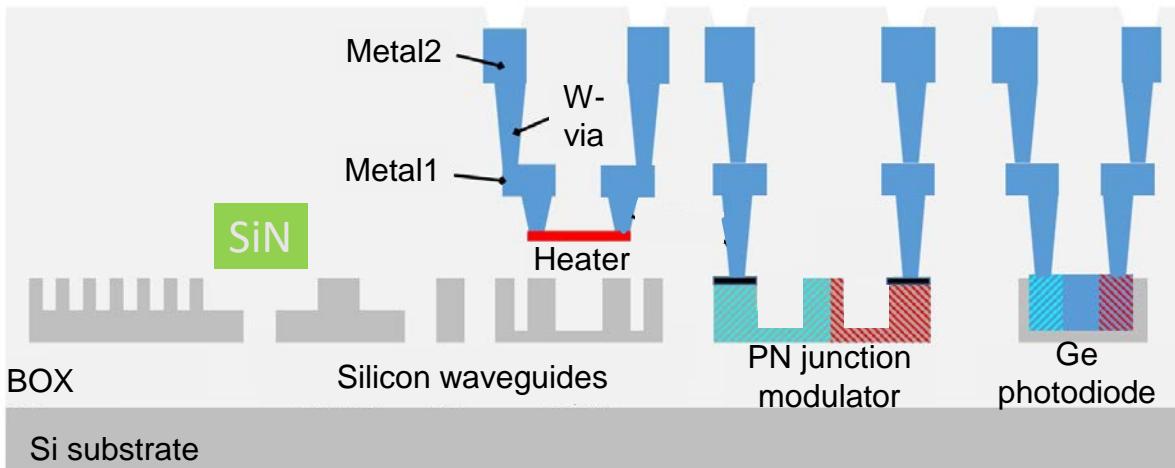
ULTRA LOW LOSS SILICON WAVEGUIDES



LOW LOSS SI WAVEGUIDES IN THE FULL PHOTONICS PLATFORM

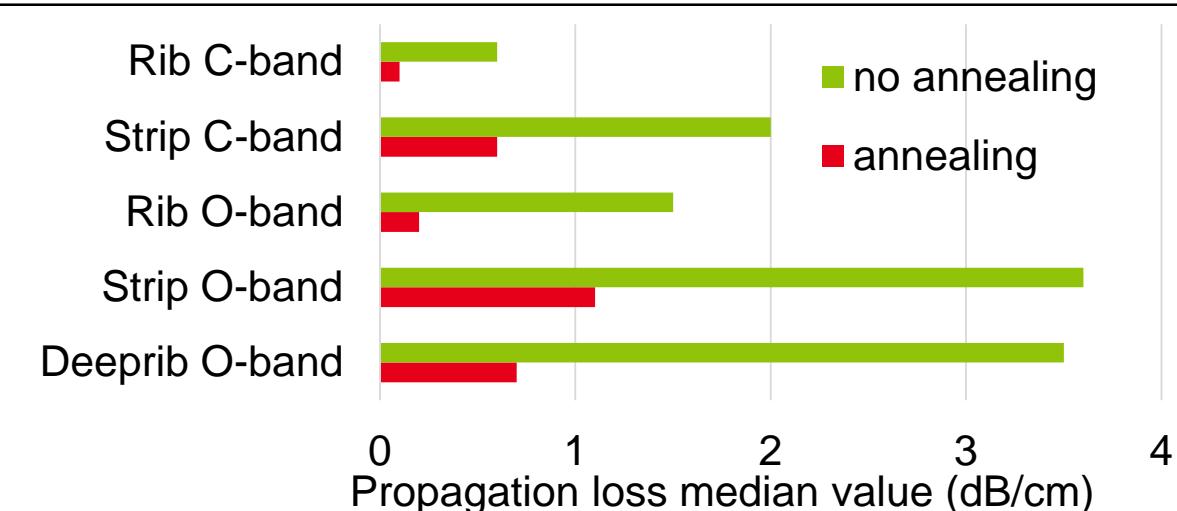
Hydrogen smoothing annealing applied on the full silicon photonics platform

- H₂ annealing leads to Si atomic surface migration
- Significant roughness reduction observed (CNRS – LTM)
- Targeting ultra-low loss on 3 types of waveguide (strip, rib and deeprib)
- Si₃N₄ hard mask on top of Si

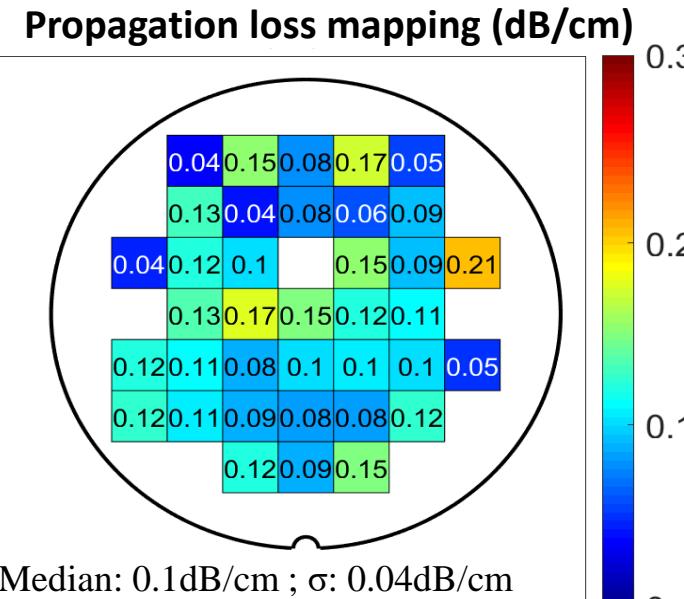
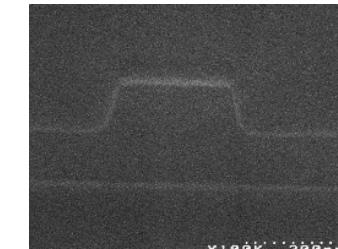


LOW LOSS SI WAVEGUIDES IN THE FULL PHOTONICS PLATFORM

- Propagation loss measurement



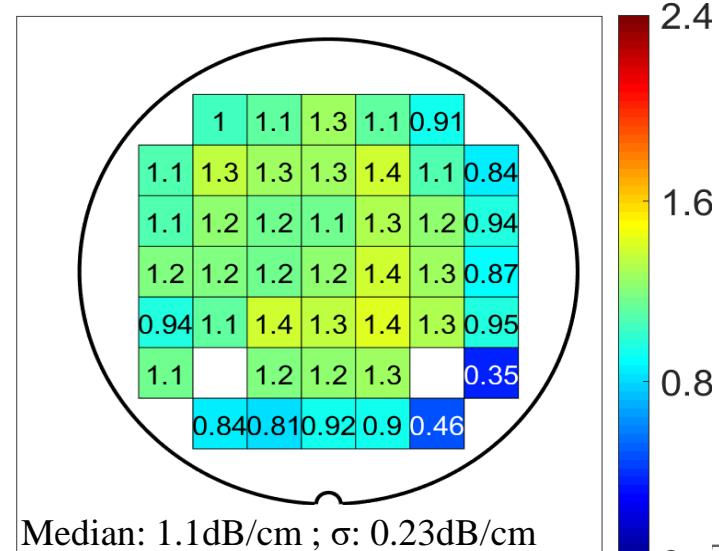
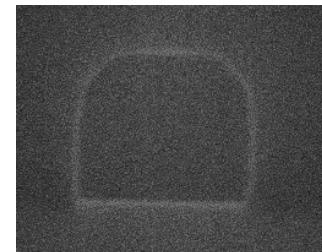
Rib
 $\lambda = 1550\text{nm}$



- Efficient sidewall smoothening
- Good wafer uniformity
- Outperform advanced immersion lithography waveguides

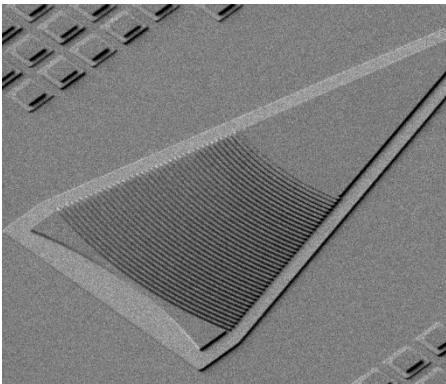
0.1dB/cm (rib) ; 1.1dB/cm (strip)
→ State-of-the-art!

Strip
 $\lambda = 1310\text{nm}$

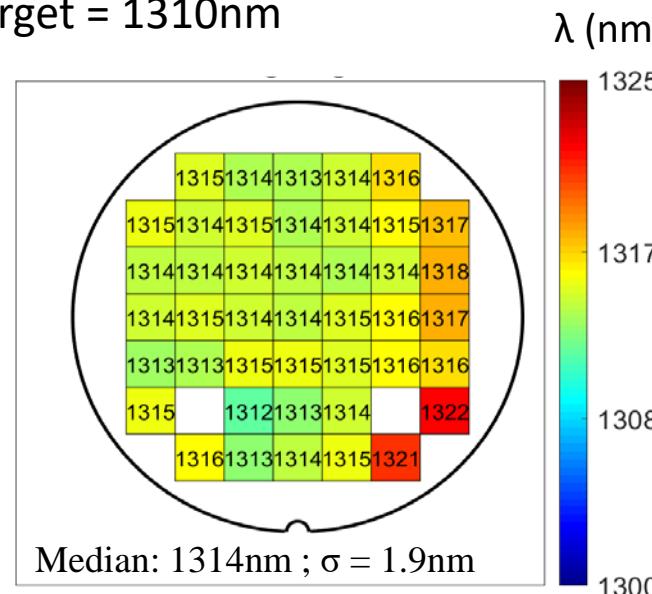


IMPACT OF ANNEALING PROCESS ON PASSIVE DEVICES

- Grating coupler central wavelength. Target = 1310nm



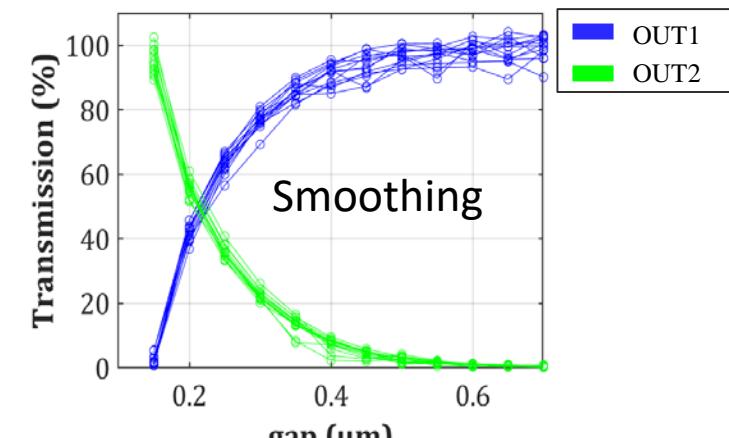
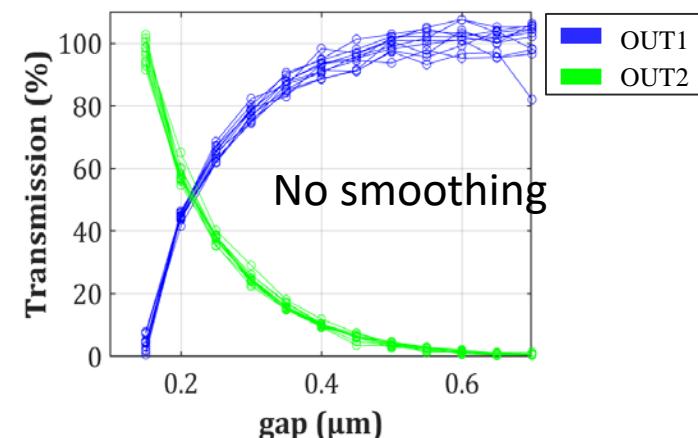
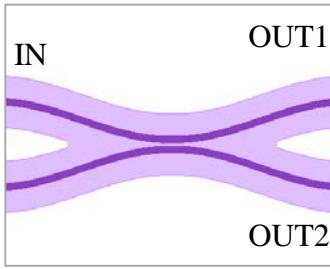
2-silicon levels apodized grating fiber coupler



- ✓ Central wavelength
- ✓ Grating coupler insertion loss = 2dB / grating

~ no impact of annealing

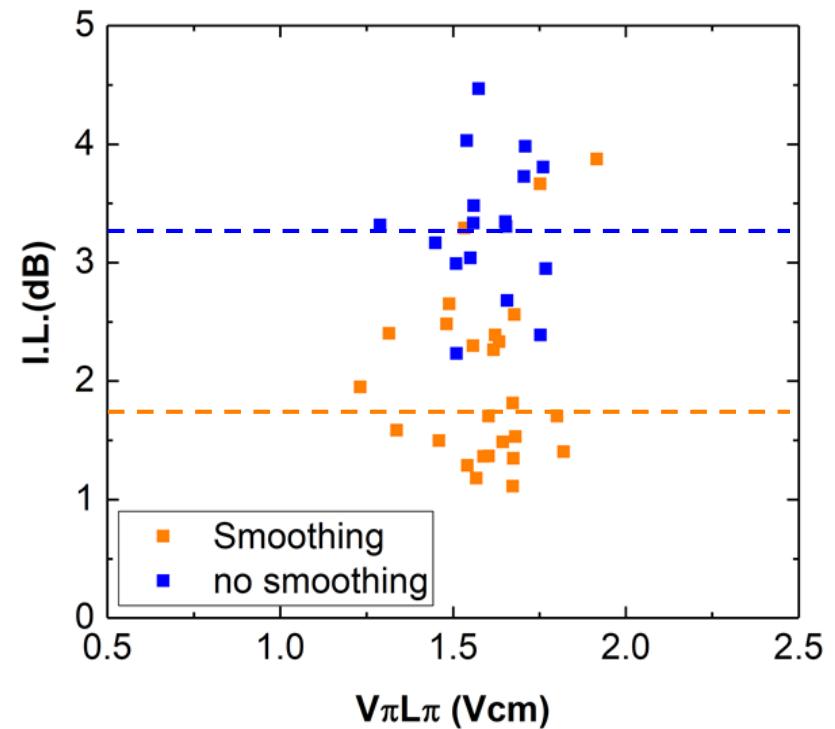
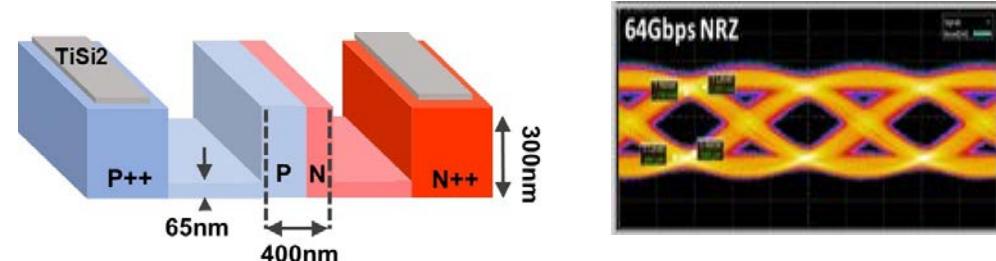
- Directional coupler transmission @1310nm



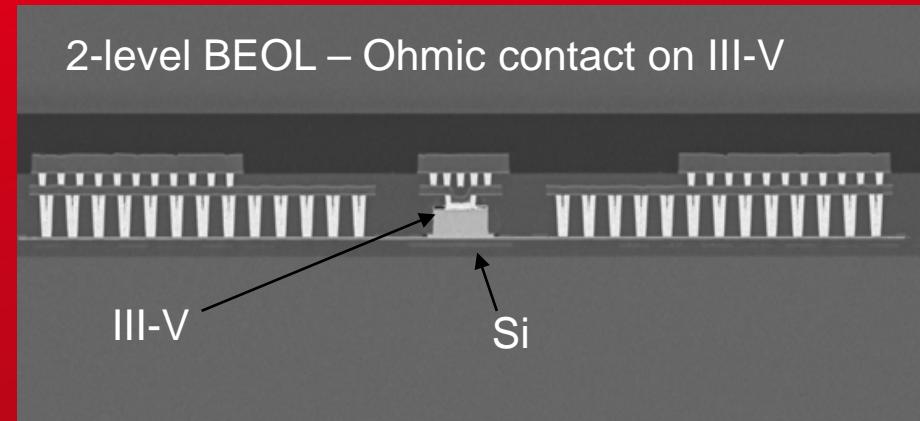
IMPACT ON MACH ZEHNDER MODULATORS (MZM)

Smoothing annealing on modulators:

- No effect of the smoothing annealing ($>800^{\circ}\text{C}$) on the P-N junction
- Efficiency preserved ($V_{\pi}L_{\pi} = 1.6 \text{ V.cm}$ with or without annealing)
- **Total loss of MZM reduced by several dBs**
(1.5dB gain with 1mm-long MZM)

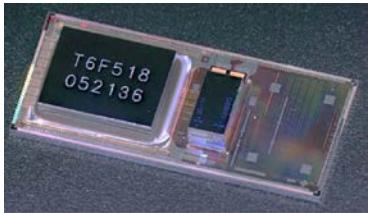


III-V LASER DIRECT BONDING INTEGRATION

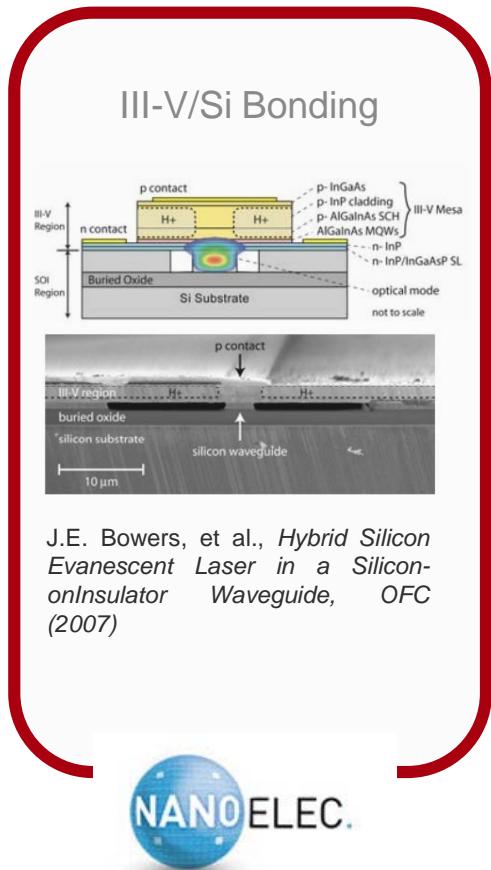


WHICH LIGHT SOURCE ON SILICON ?

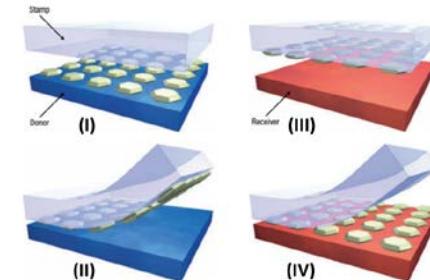
Assembly of already processed III-V laser



Luxtera's silicon photonics Optical Engine (100G TX+RX PSM-4)

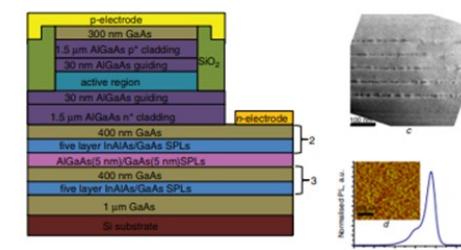


Transfer printing



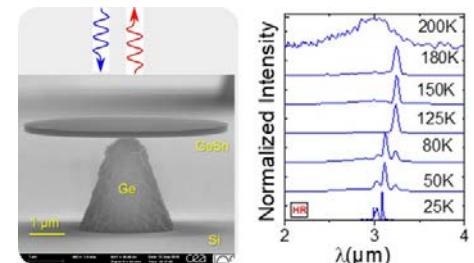
M. A. Meitl, et al, *Transfer printing by kinetic control of adhesion to an elastomeric stamp*, *Nature Materials* **5**, 33–38 (2006)

Direct epitaxy of III-V on Si



S.M. Chen, et al, *1.3 μm InAs/GaAs quantum-dot laser monolithically grown on Si substrates operating over 100°C*, *Electronics letters*, Vol. 50 No. 20 pp. 1467–1468 (2014)

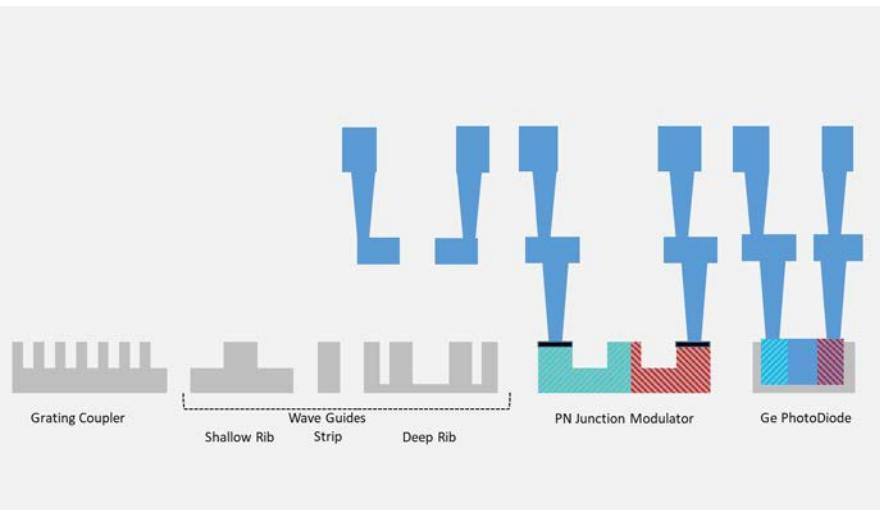
Ge(Sn) laser on Si



V. Reboud et al., *Optically pumped GeSn micro-disks with 16% Sn lasing at 3.1 μm up to 180K*, *Appl. Phys. Lett.* **111**, 092101 (2017).

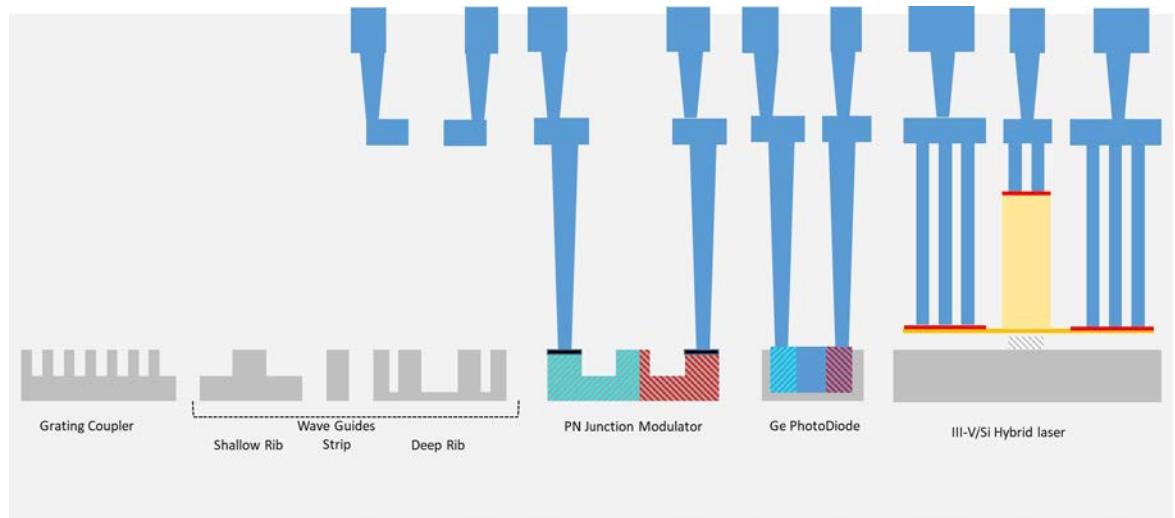
TECHNOLOGY – LASER INTEGRATION IMPACT

Si Photonic Plateform Core Process



- 310nm SOI – 2 μ m BOX
- 193nm DUV lithography
- Multilevel silicon patterning
- 8 Implantations levels
- Selective Germanium epitaxy
- Silicide
- Metal heater
- Planarized BEOL
- 2 AlCu routing levels
- UBM for Cu pillar assembly

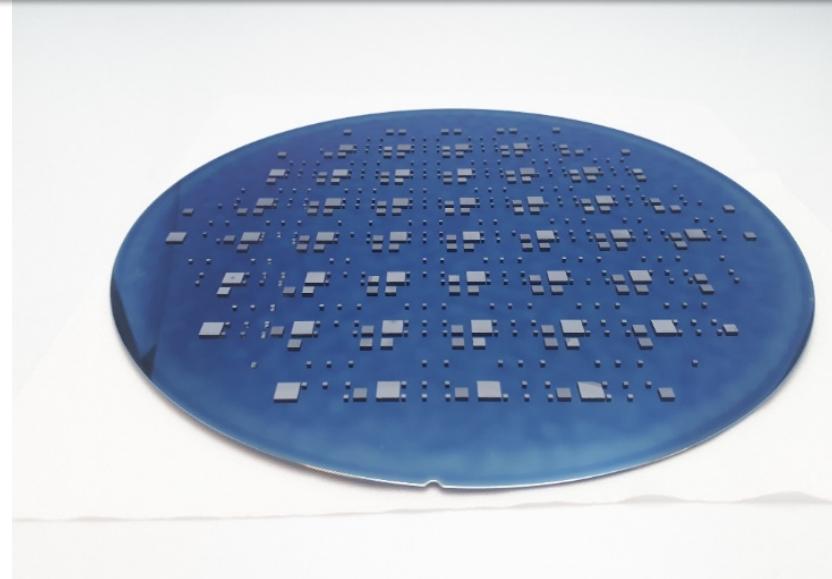
CMOS Compatible III-V/Si Integrated Laser



- Collective die bonding
- Additional Laser process steps cmos compatible:
 - No noble metals for III-V contacts
 - Conventional patterning steps (no lift-off)
- Thick M1 to Silicium contact module
- Localized Si thickening on 310nm SOI:
 - Damascene process with Si-Amo or selective Si-epi
- Planarized multi-metal level BEOL
- Additional thermal budget due to laser integration < 600°C

LASER ON SI LARGE SCALE INTEGRATION: DIE BONDING

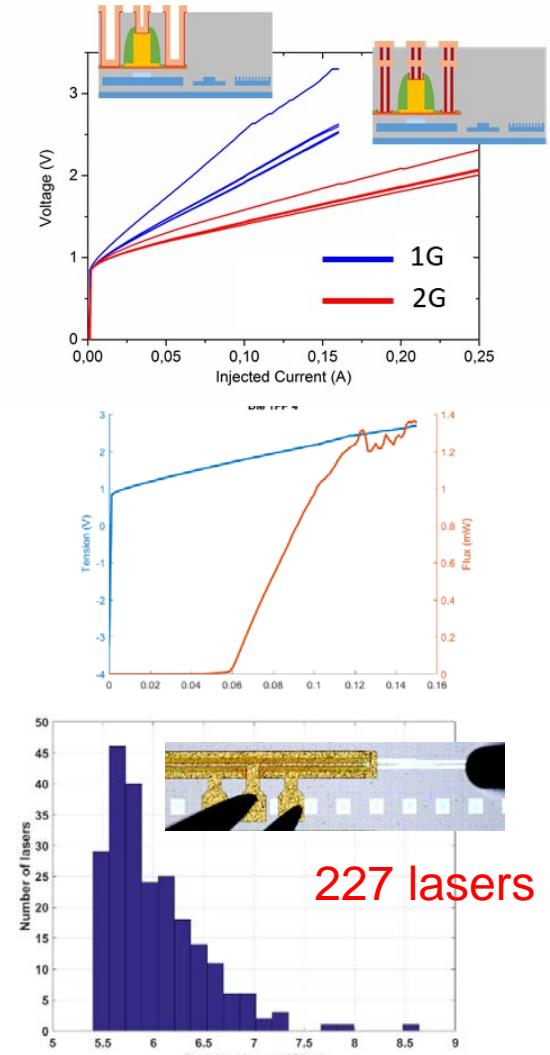
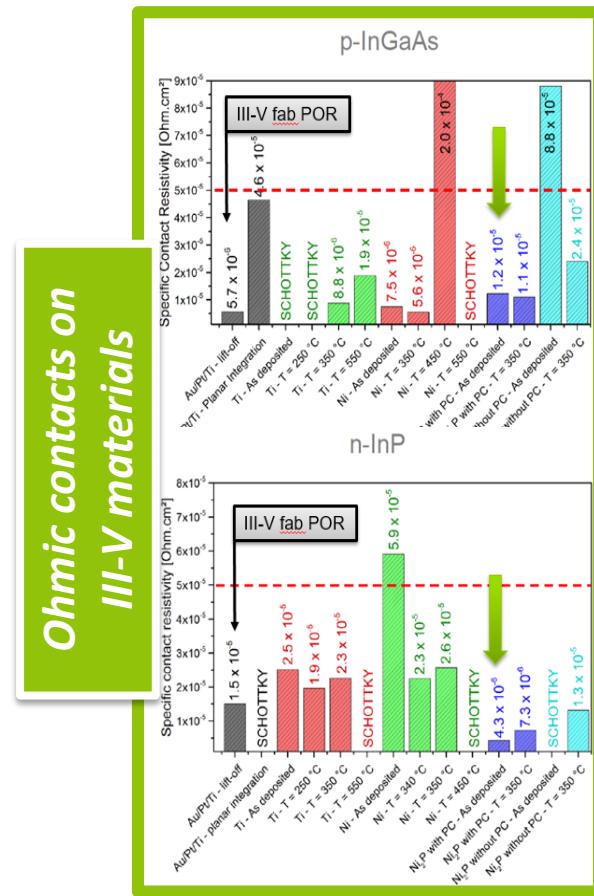
Development of automated die bonding of III-V/SOI



Collective die Bonding with adhesive film

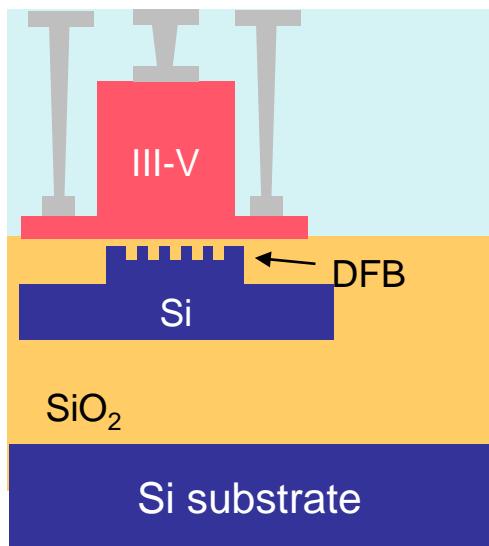
- + Process validated for InP die
- + Process compatible with die thickness variations up to 50 μm
- + Compatible with multidie bonding
- + Minimum Die Size 1x1mm²
- + Die spacing 400 μm
- + Scalable to 300mm wafers

Development of efficient CMOS friendly BEOL / III-V

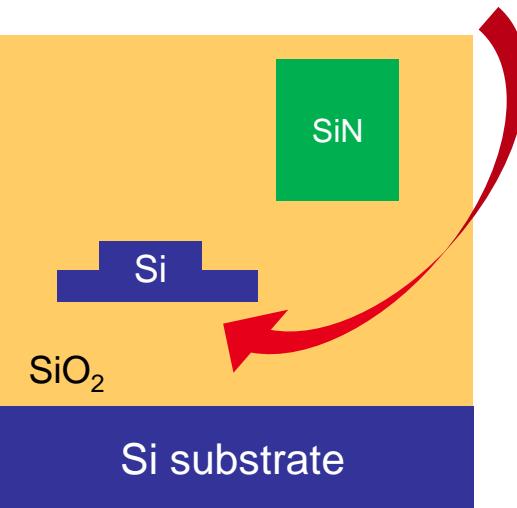


III-V INTEGRATION ON THE SI/SiN PLATFORM

Si/III-V integrated platform

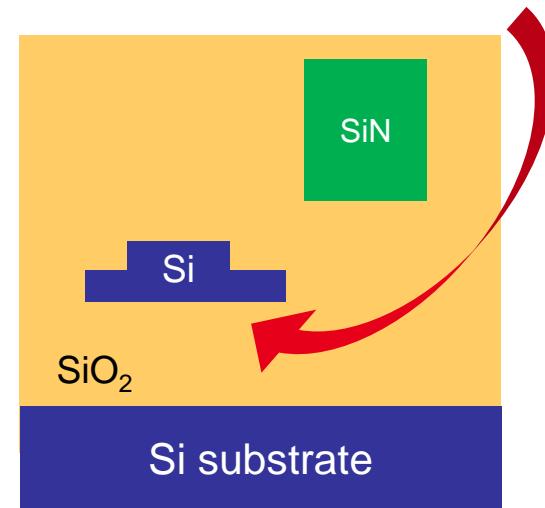


Si/SiN platform

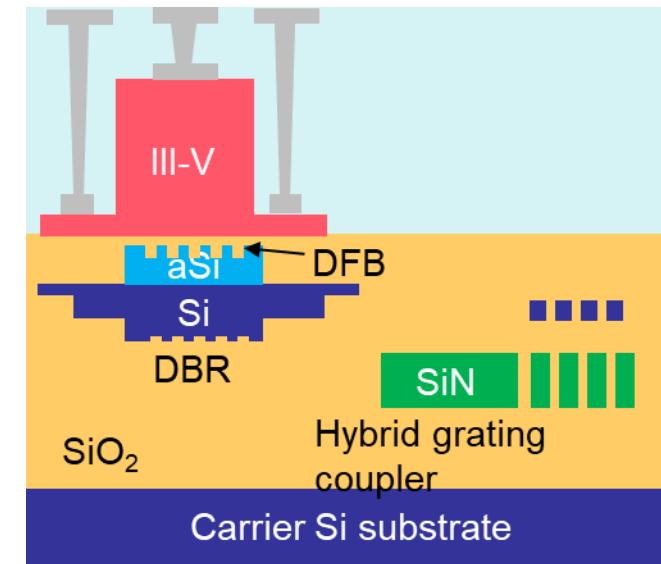
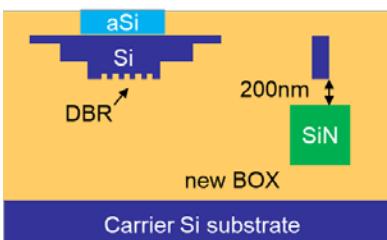
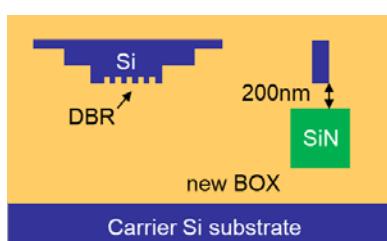
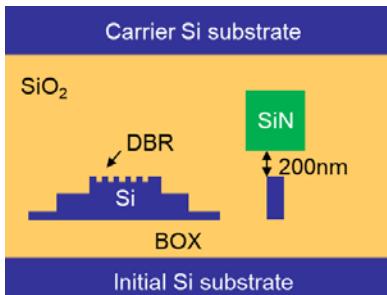
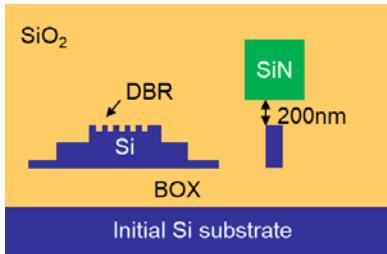


- III-V 100nm on top of Si
- Si is 500nm thick
- Si/III-V coupling

Solution: III-V in the backside



- SiN is 200nm on top of Si
- Si is 300nm thick
- Si/SiN coupling

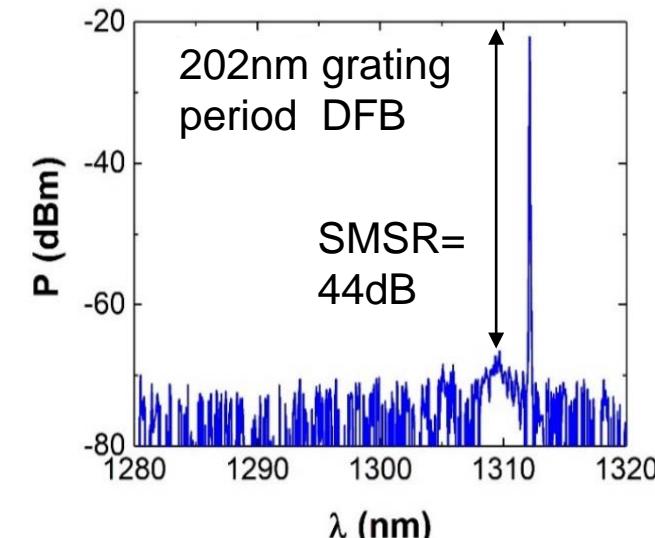
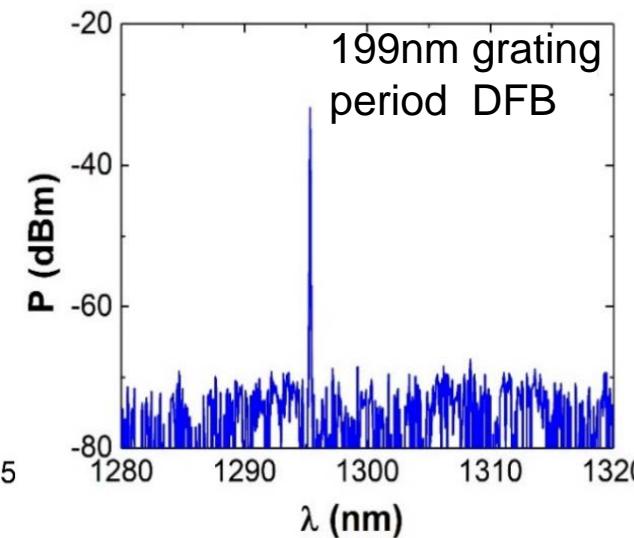
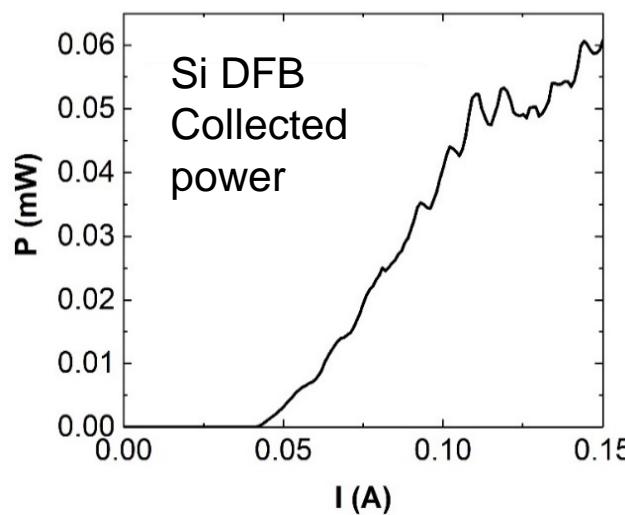
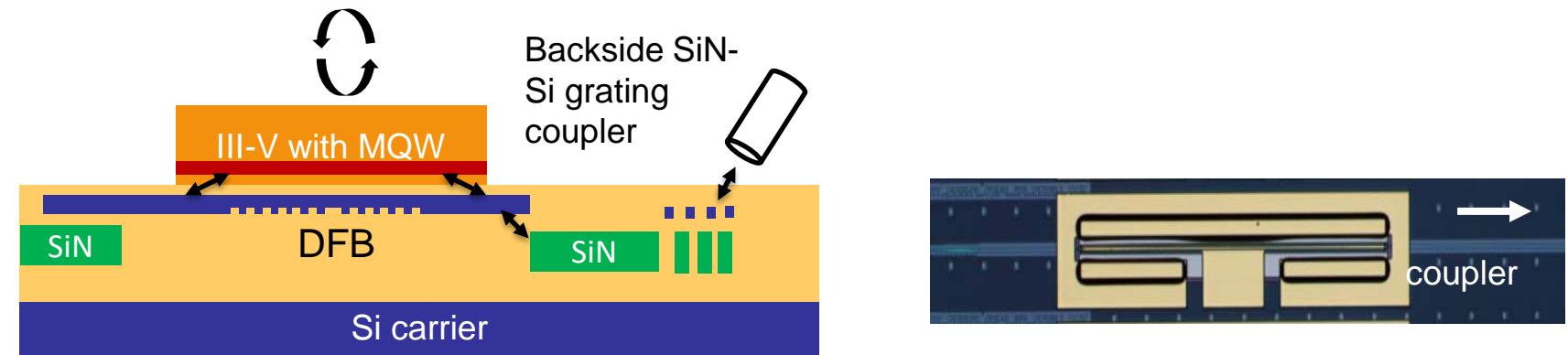


Backside integration of III-V epitaxy on the backside of the Si/SiN platform

SCINTIL spin-off

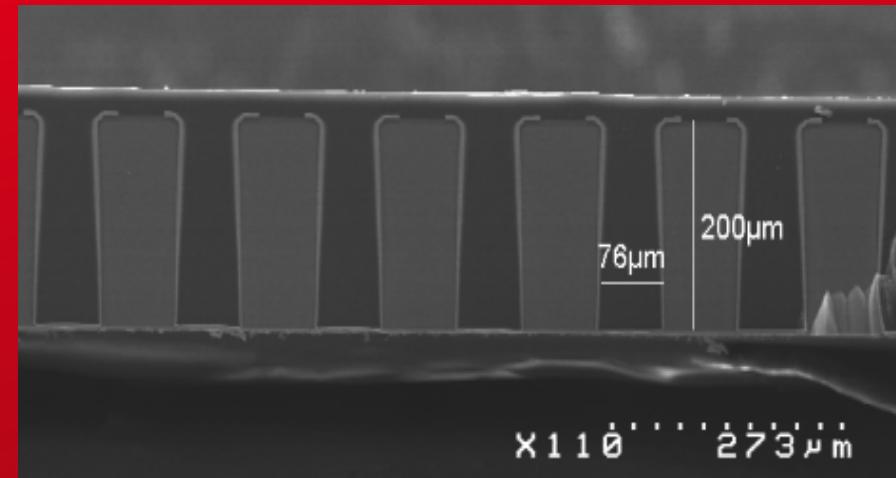
III-V/SI LASER ON THE SI/SIN PLATFORM

- III-V/Si hybrid laser with backside integration
- DFB type laser (DFB grating in Si)
- Gain length = 400μm
- Off-chip coupling with SiN/Si grating coupler

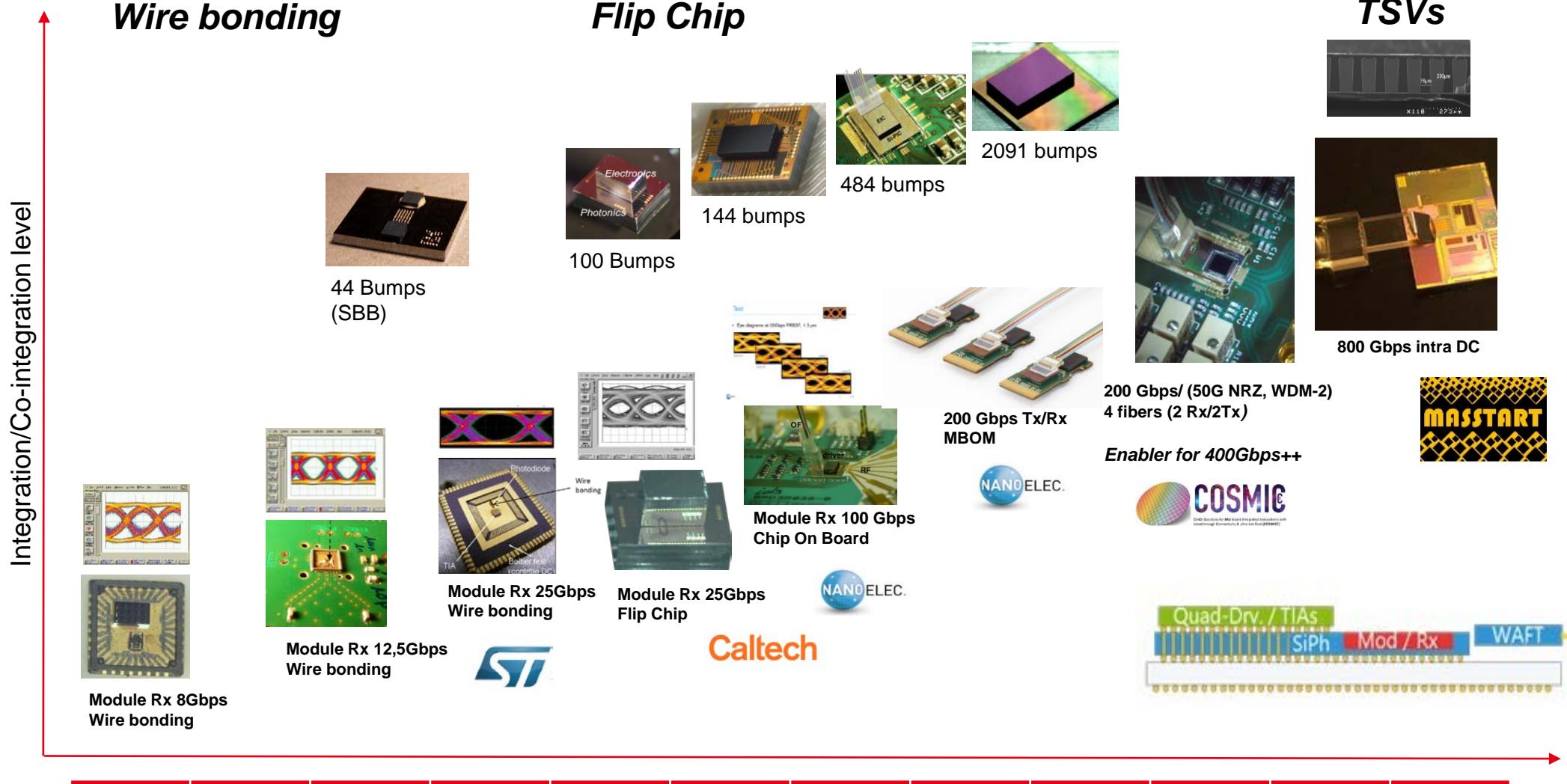


- ✓ 2-λ DFB: 1295nm & 1312nm
- ✓ Single mode émission
- ✓ SMSR = 44dB
- ✓ Power up to 0.8mW in waveguides

ADVANCED PACKAGING



HIGH SPEED MODULES USING LETI PLATFORM



- **3D Integration**

- **TSV last**

- Backside Etching
- 2 μ m Cu liner

- **TSV mid**

- Frontside Etching
- Grinding to 100 μ m thickness
- Study of stress/strain on photonics layers

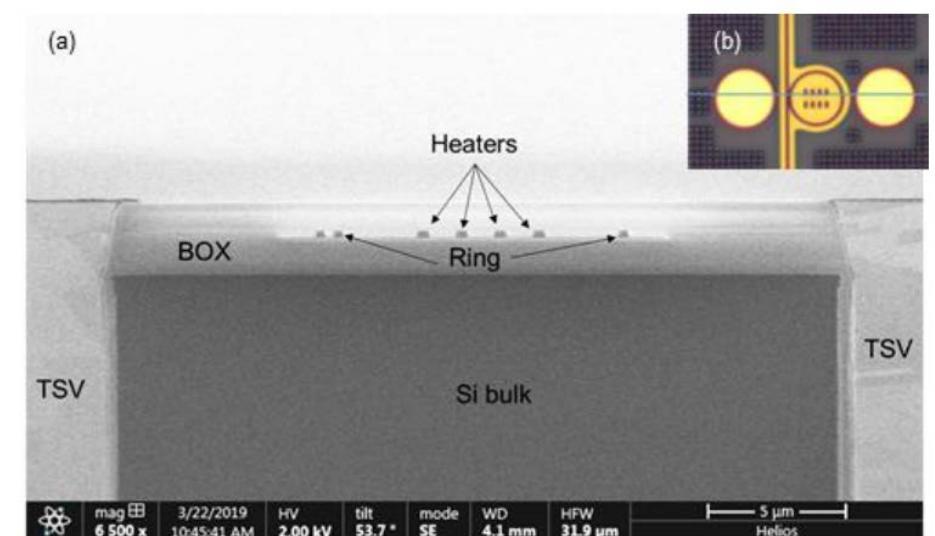
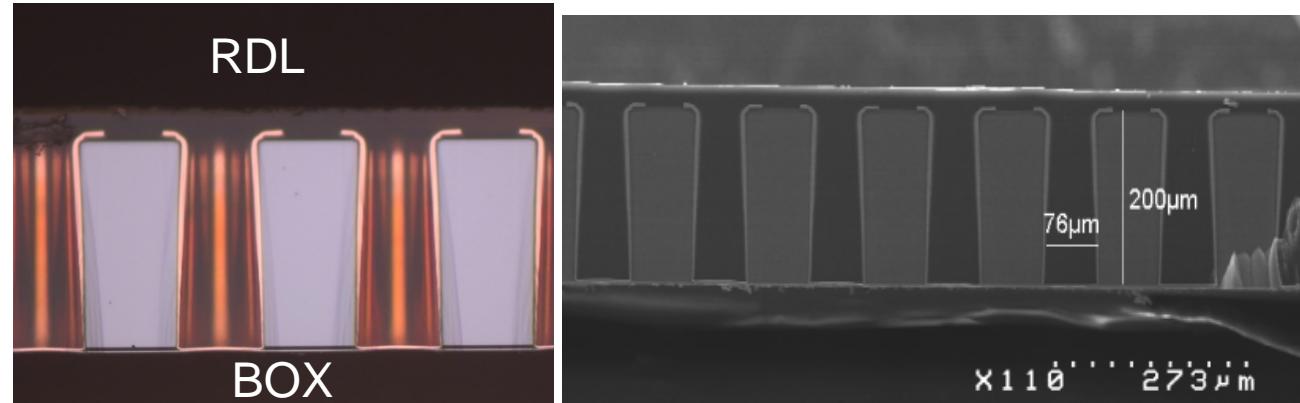


Fig. 4. a) SEM cross section of the TSV-surrounded ring before BEOL, b) optical top view of the ring and its TSVs and corresponding cross section plane

CONCLUSION

Silicon Photonics is now part of commercial modules for 100G / 400G inter/intra DC links

800G + applications are setting new challenges

Increased data rate :

- Requiring PAM-4 and WDM
- ***SiN add-on*** enhances existing libraries with broadband and Mux athermal devices

Increased density:

- Following the co-packaging roadmap
- ***3D packaging*** is a must

Increased complexity:

- Increased size of circuits
- Require ***low loss waveguides*** and photonics EDA tools

All these challenges (+ laser integration) are addressed by CEA-LETI through add-on plugged on an existing standard Silicon Photonics Platform (200mm ready, 300mm available in 2021)

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Leti Photonics team



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