TSV integration into silicon photonics interposer for next generation transceiver PICs

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Data Center Interconnects – Towards Mass Manufacturing
online / October 6th 2020 / 4 – 7pm

TSV integration into silicon photonics interposer for next generation transceiver PICs

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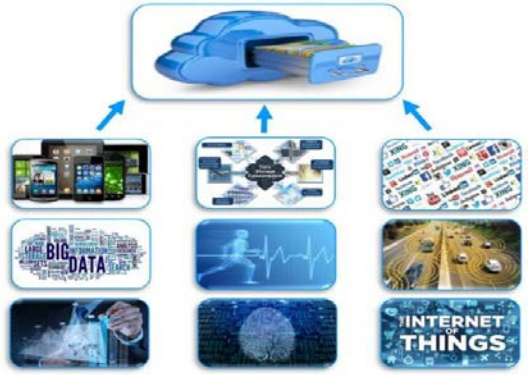
Fraunhofer Institute for Reliability and Microintegration (IZM), Berlin

Photonics days Berlin Brandenburg 2020

Data Age - Global datasphere by 2025



163ZB
Amount of **data** that will be **created annually**

20%
Amount of **life-critical data** in datasphere

4800/day
Amount of one persons **interaction** with **IoT devices**

25%
Amount of created **real-time data** in datasphere

5.2ZB
Amount of data that subject to **data analysis**

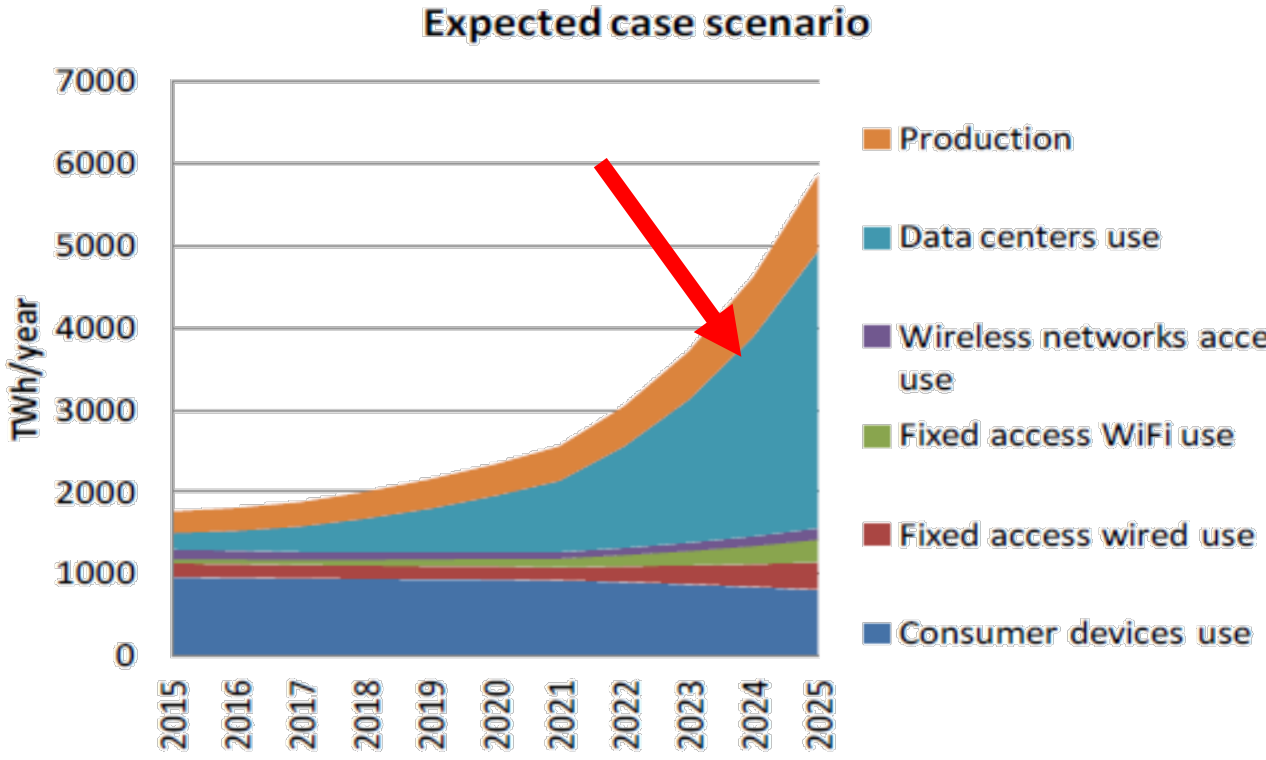
1.4ZB
Amount of analysed data touched by **AI / cognitive systems**

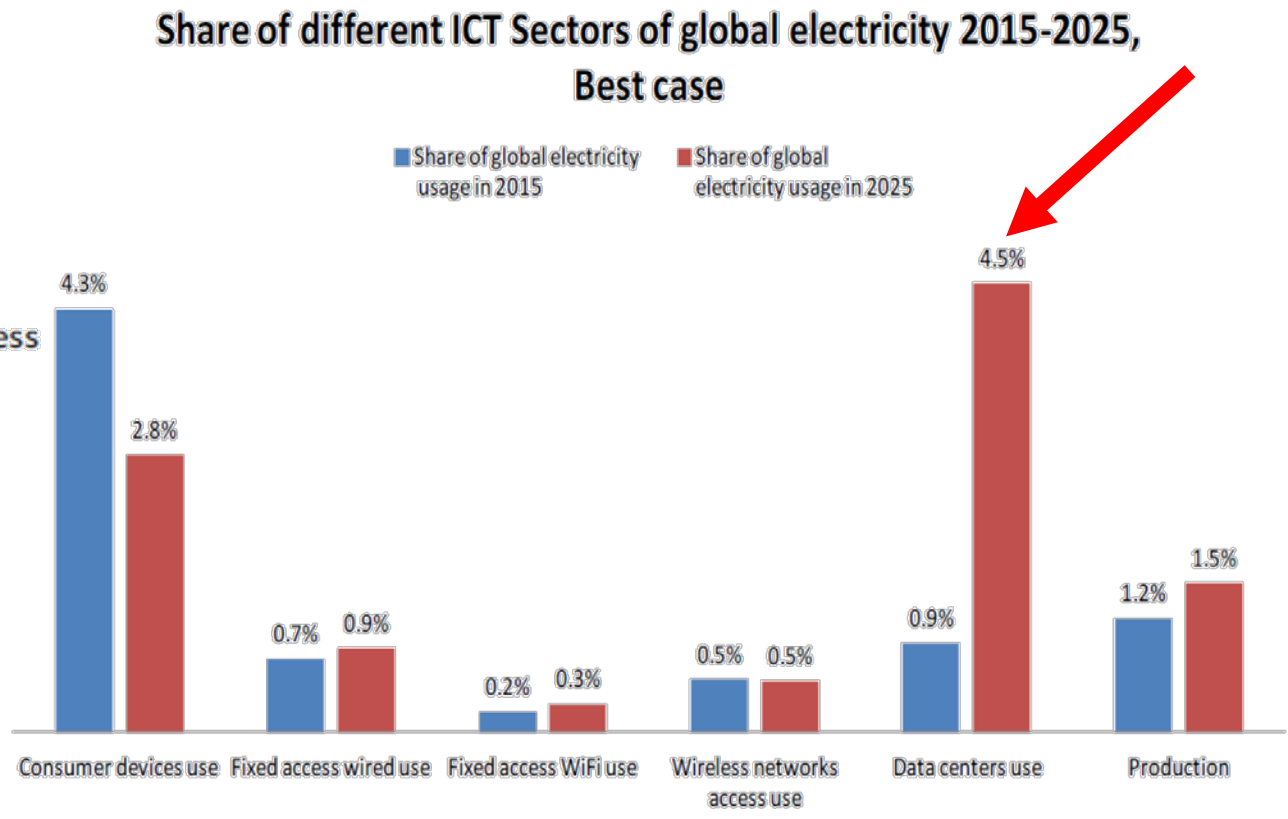
90%
Amount of **data** in datasphere require **security**

Source: IDC, Seagate

1 zettabyte : 10^{21} bytes

The Downside

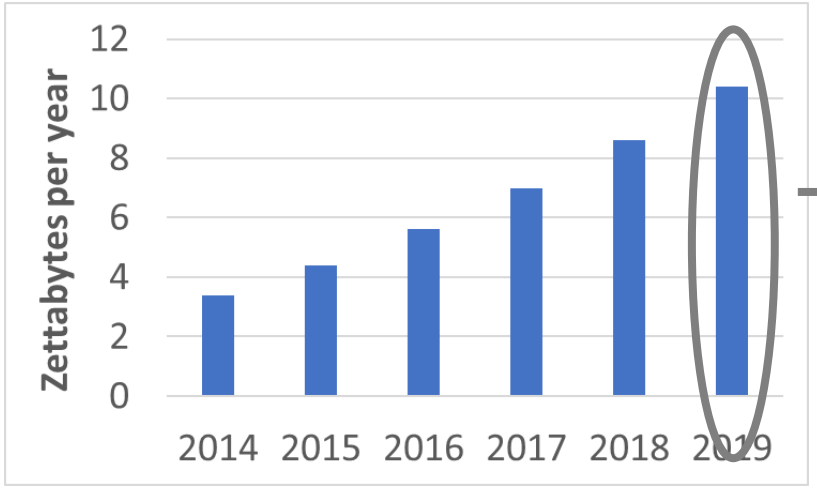




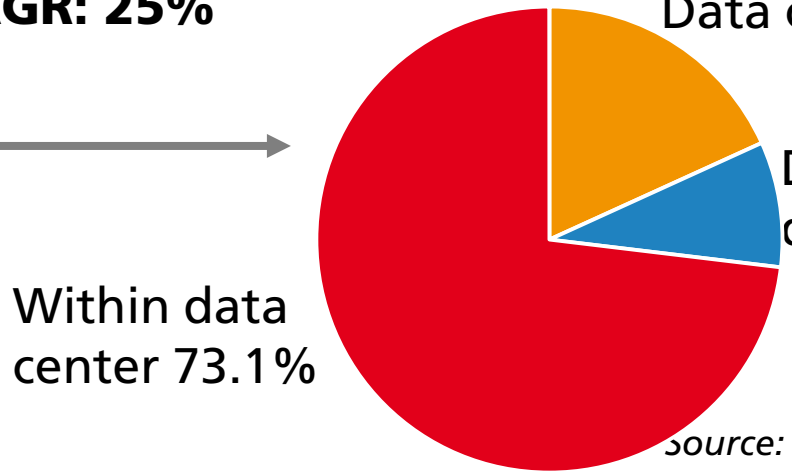
Source: Total consumer power consumption forecast, Dr. Anders S. G. Andrae (Huawei), Nordic Digital Business Summit, October 2017

Motivation – Data center traffic growth

Forecast 2014:

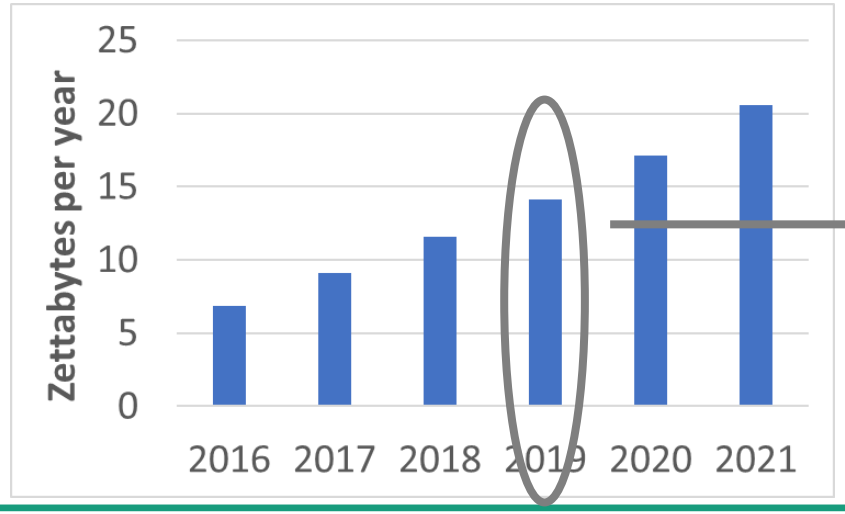


CAGR: 25%

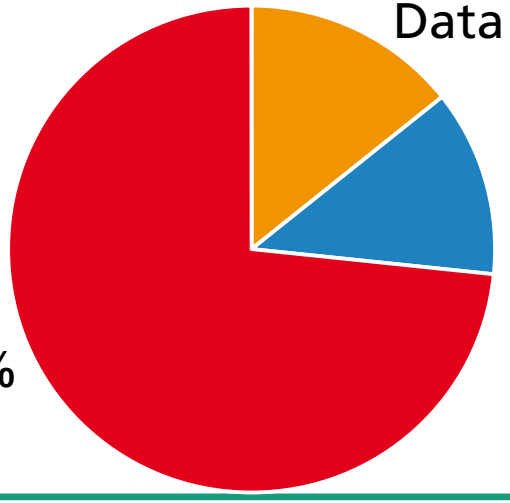


Source: Cisco Global Cloud Index 2014

Forecast 2018:

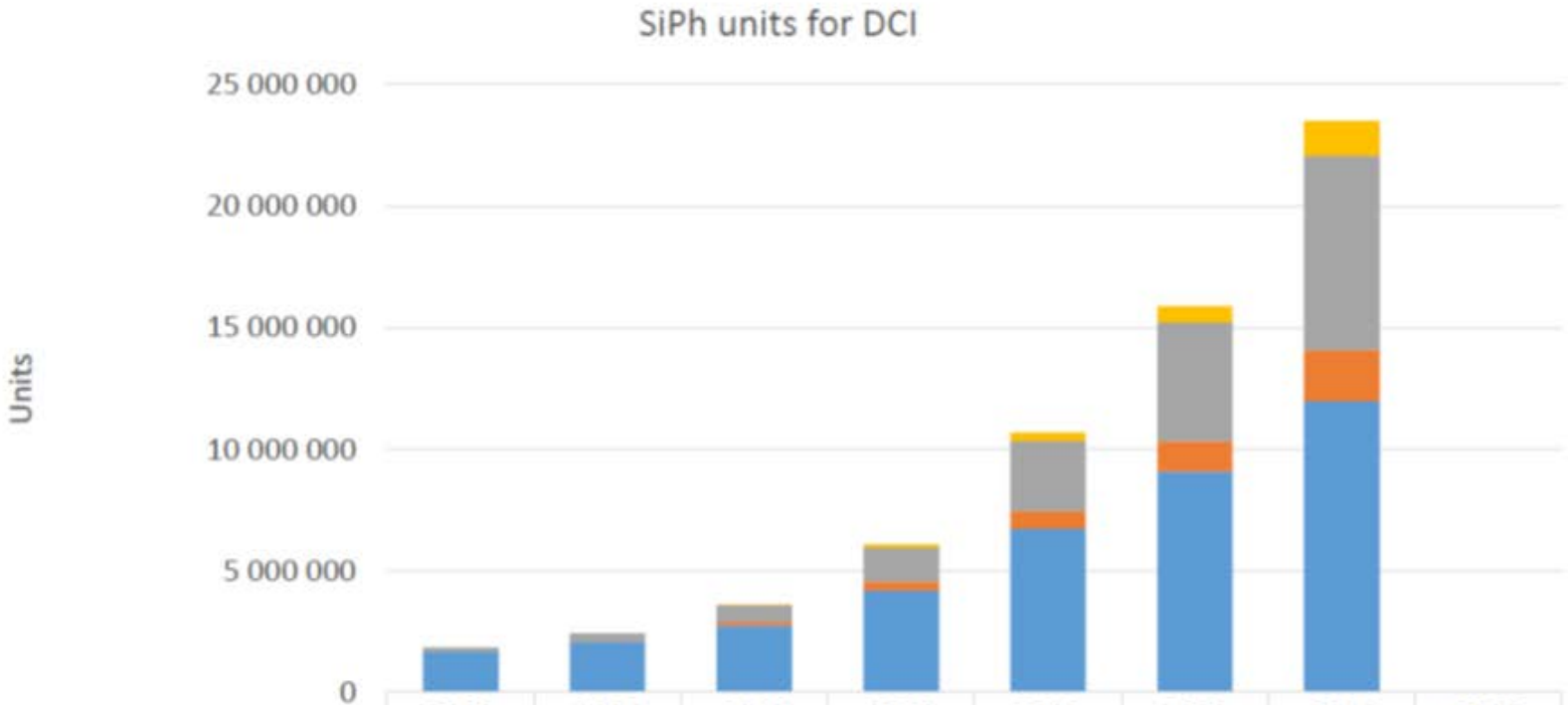


CAGR: 24.7%



Source: Cisco Global Cloud Index 2016-2021 (2018)

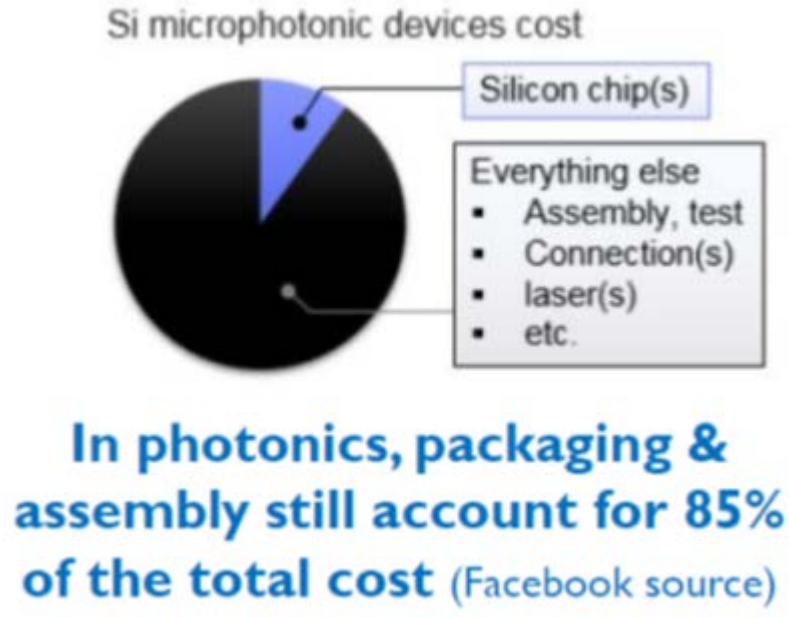
Silicon Photonics Chip Forecast for DCI



	2018	2019	2020	2021	2022	2023	2024	CAGR
200/400G units CWDM4	0	0	36 241	121 524	320 234	667 040	1 409 587	149,7%
100G units CWDM4	185 000	362 876	688 575	1 397 521	2 882 109	4 891 627	7 987 660	87,3%
200/400G units PSM4	0	0	144 963	364 571	747 213	1 238 789	2 114 380	95,4%
100G units PSM4	1 665 000	2 056 299	2 754 301	4 192 563	6 724 921	9 084 450	11 981 48	38,9%

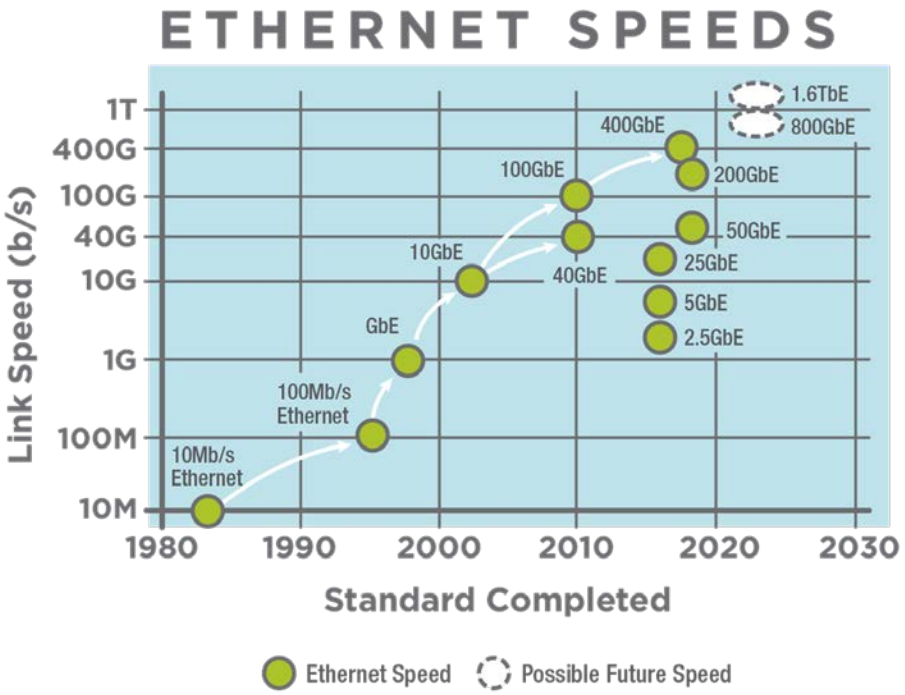
Source: Yole

Photonics Packaging Key Challenges

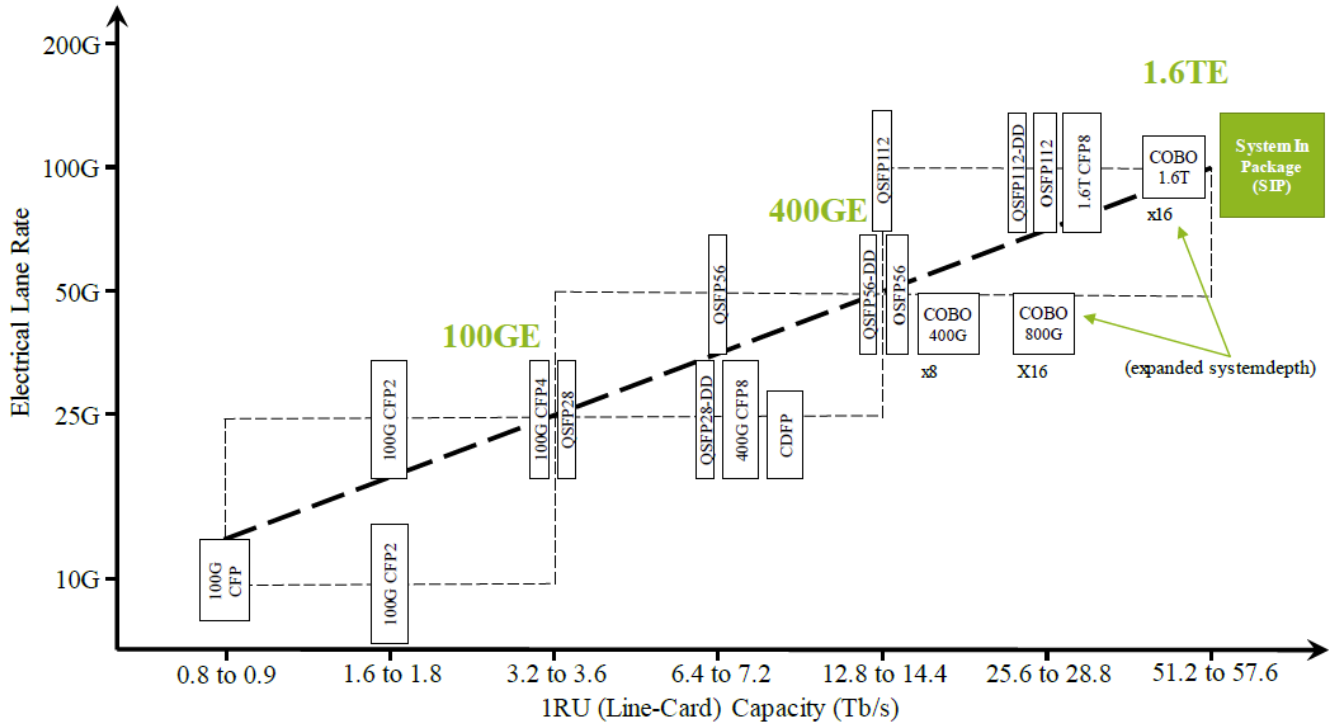


- High precision placement for fiber **alignment** for SM
- Delicate parts **handling**
- Different **die attach** technologies for assembly
- **Testing**
- **Standardization**
- Reliability
- Small and odd shape devices
- **High cost**

Ethernet speed – Historical Data and Forecast



- 100G proliferating
- 400G ramp up after 2021



- Next stop, 800G and 1.6T
- Road >400G includes COBO and co-packaging

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MASSTART surpasses the cost metric threshold by using enhanced and scalable techniques

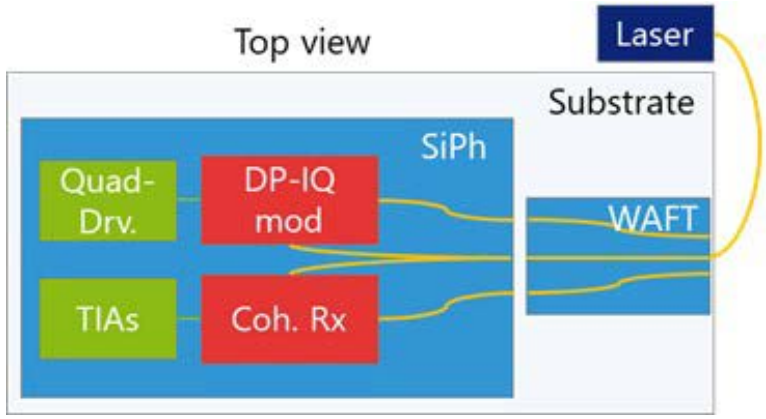
- Glass interface based laser/PIC and fiber/PIC **coupling** approaches, leveraging **glass waveguide** technology to obtain spot size and pitch converters in order to dramatically increase optical I/O density, while facilitating automated assembly processes,
- 3D packaging (**TSV**) enabling backside connection of the high speed PIC to a Si carrier,
- A new generation of **flip chip bonders** with enhanced placement in a complete assembly line compatible with Industry 4.0 which will guarantee an **x6 improvement in throughput**
- **Wafer-level evaluation** of assembled circuits with novel tools that will reduce the characterization time by a factor of 10, down to **1 minute per device**.

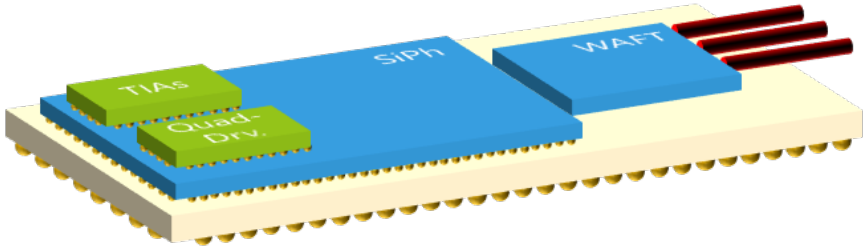
- 4-channel PSM4 module in QSFP-DD format with 400G aggregate bit rate,
- 8-channel WDM module in a QSFP-DD format with 800G aggregate bit rate,
- 16-channel WDM on-board module delivering 1.6Tb/s aggregate line rate,
- A tunable single-wavelength coherent transceiver with 600Gb/s capacity following the DP-64QAM modulation format on 64Gbaud/s line rate.

MASSTART – Consortium as a whole

- System providers
- Photonic Assembly & Testing
- Design House & Technology consultancy
- Technology providers

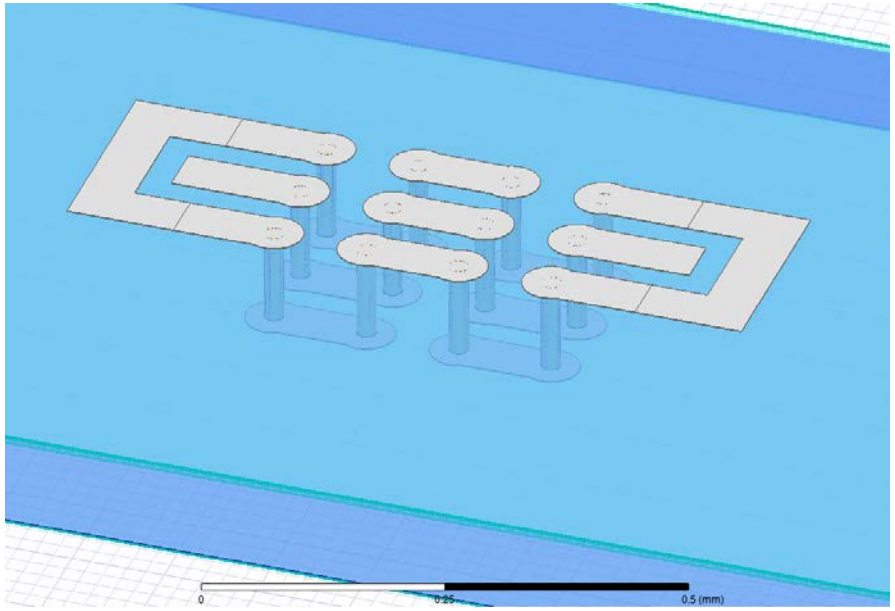
MASSTART Coherent Transceiver Packaging

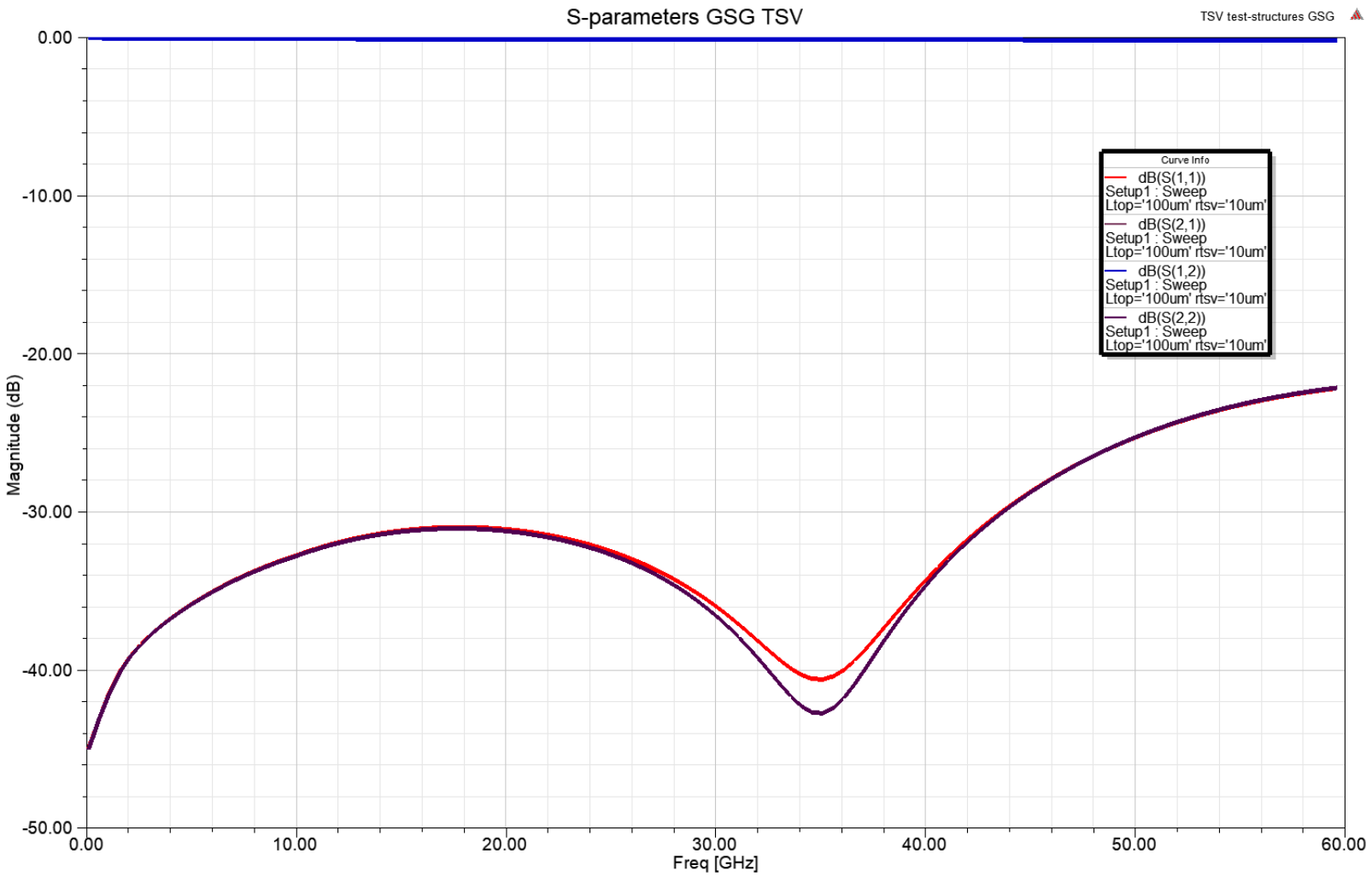




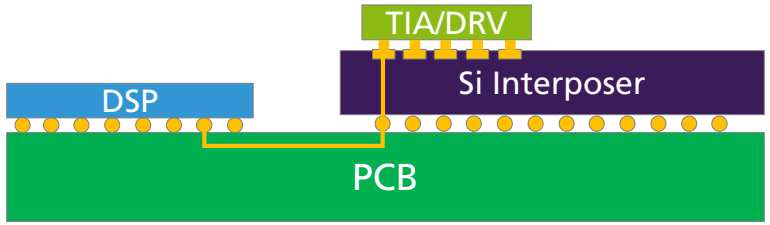
- ✓ Glass interface based laser/PIC and fiber/PIC coupling approaches
  - → obtain spot size and pitch converters
  - → increase optical I/O density, automated assembly processes
- ✓ 3D packaging using TSV enabling backside connection of the high speed PIC to a Si carrier
- ✓ New flip chip bonders with enhanced placement
  - → improvement in throughput
- ✓ Wafer-level evaluation of assembled circuits with novel tools
  - → reduce characterization time

TSV Test-structures GSG



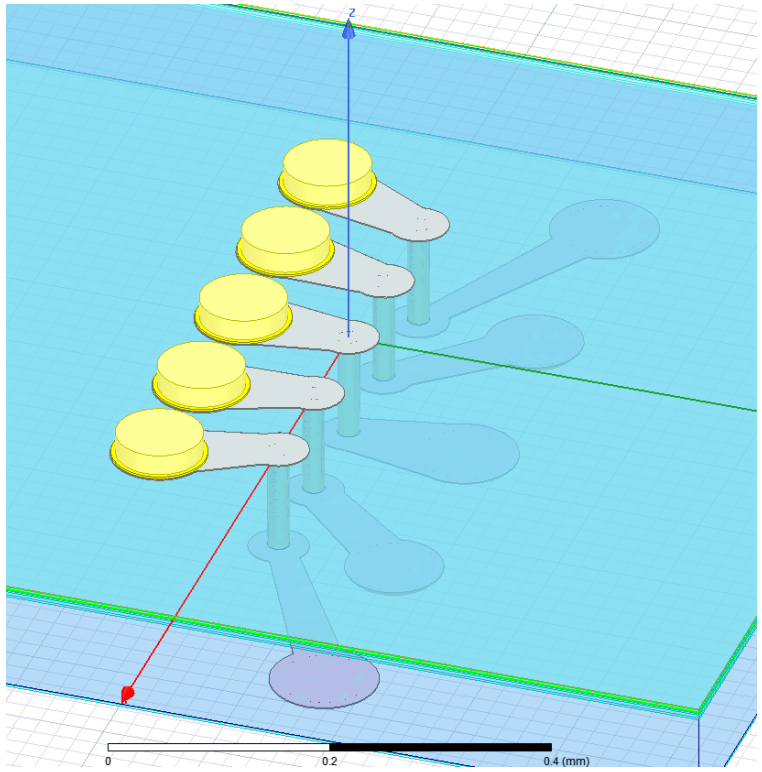


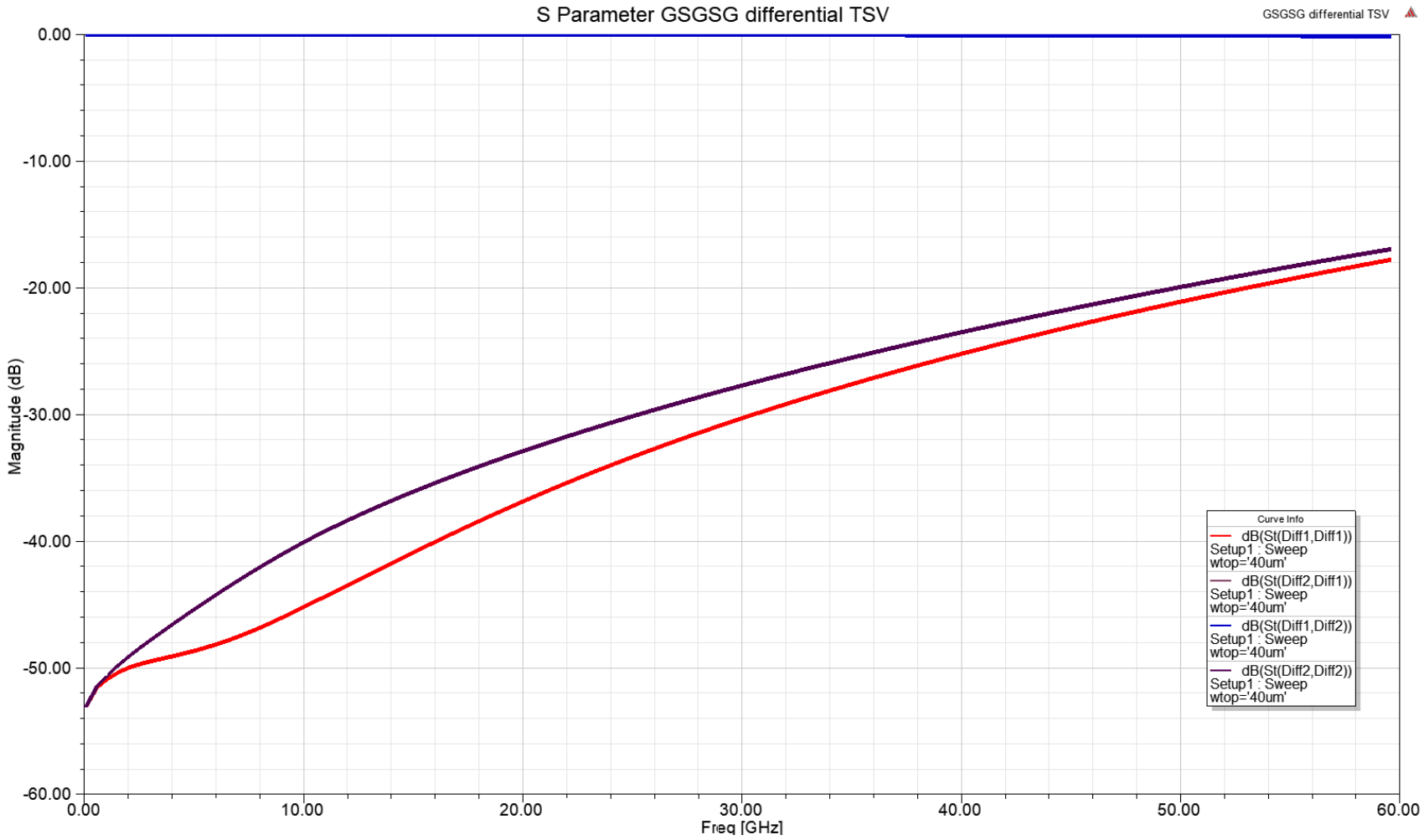
GSGSG TSV Application Scenario



Required to connect:

- Driver/TIA chips assembled on top of the Interposer
- DSP chip assembled on the PCB





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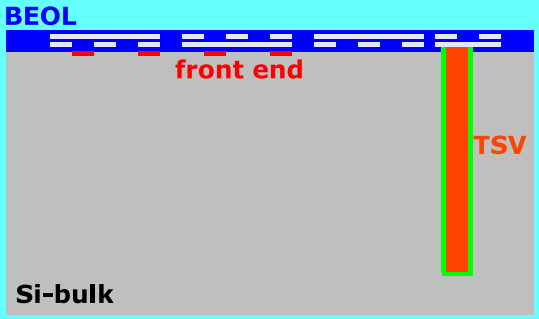
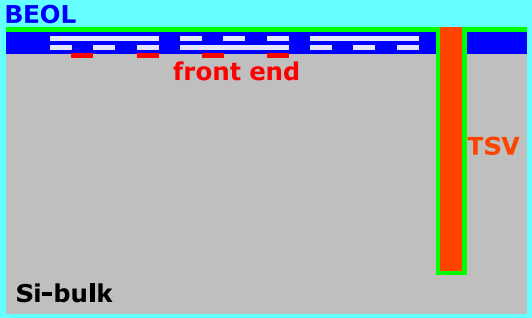
TSV Integration Schemes

Via first or middle;

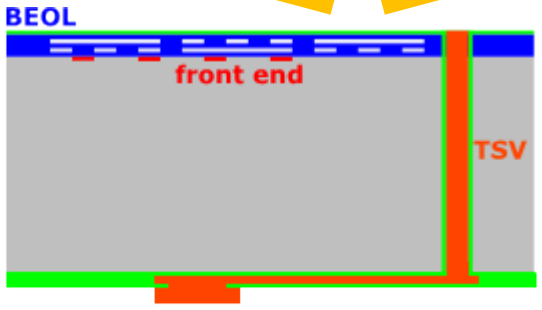


- TSV integration before FEOL or after FEOL / before BEOL
- Processes established at IDMs

Via last;

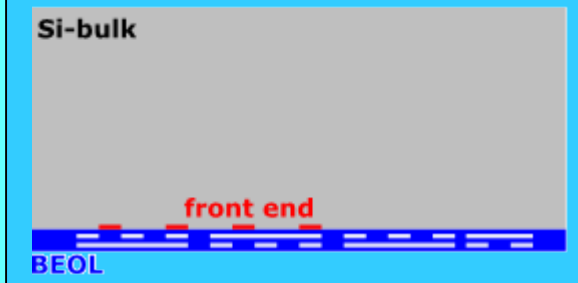


- TSV integration after complete wafer processing
- TSV through thick BEOL oxide
- Requires keep out zones in FEOL and BEOL for TSV integration

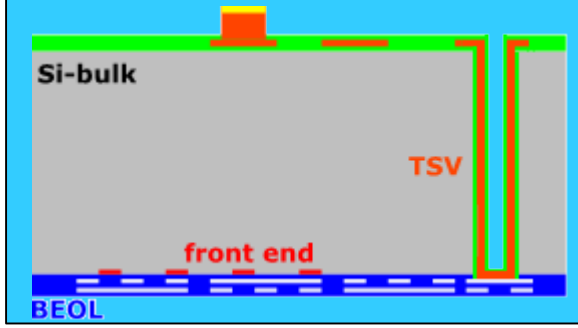


- Support wafer bonding
- Wafer backside thinning
- TSV reveal
- Backside RDL and bump formation
- Support wafer de-bonding

Back Side Via last



- TSV integration after complete wafer processing
- Requires landing pads in BEOL for prepared TSV connection



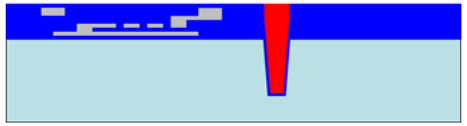
- Support wafer bonding
- Wafer backside thinning
- TSV formation with acess to landing pads
- Metall liner and back side RDL formation
- Support wafer de-bonding (if required)

Front and Back Side Processes for TSV, RDL and IO formation

1. **Original wafer condition**
   - Original IO pads opened
   - keep out zones in FEOL and BEOL (red circle)

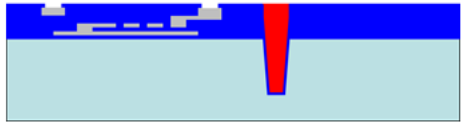
2. **TSV process**

   (Litho mask required-->layer 10 in current TRX8 layout)
   - original IOs pads are covered with passivation layer after TSV process



3. **Passivation opening over original IO pads**

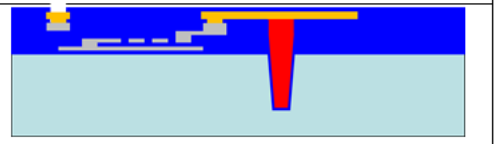
   (Litho mask required-->layer 8 in current TRX8 layout)



4. **Front side RDL formation (1µm Al)**

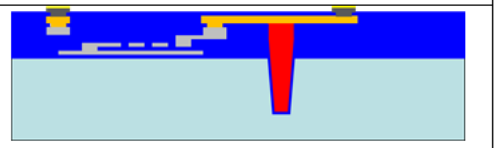
   (Litho mask required-->layer 11 in current TRX8 layout)
5. **RDL passivation (1µm CVD Oxide / Nitride)**

   (Litho mask required-->not foreseen in TRX8 layout)

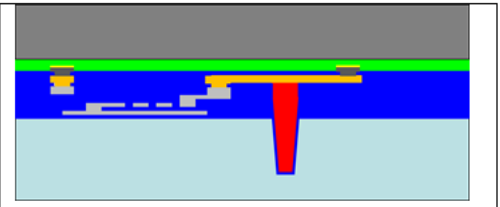


6. **Front side pad metallization**

   (Litho mask required-->not foreseen in TRX8 layout)
   - original IOs can be covered with pad metallization
   - pad metallization to be located at all positions were passivation is opened
   - pad formation on top of TSVs not allowed

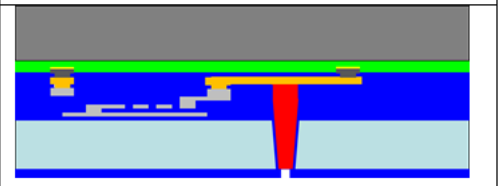


7. **Temporary carrier bonding**



8. **Back grinding / TSV reveal**
9. **Back side passivation (1µm CVD Oxide / Nitride)**

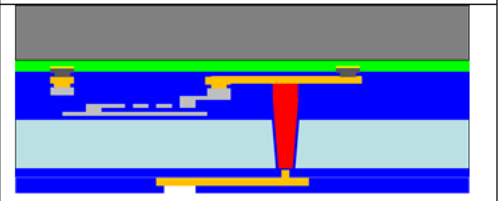
   (Litho mask required-->layer 9 in TRX8 layout)



10. **Back side RDL (1µm Al)**

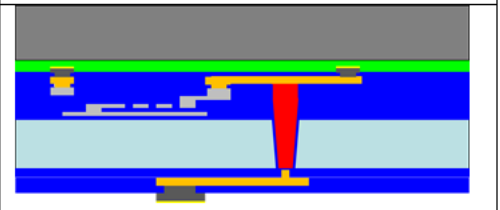
    (Litho mask required-->layer 21 in TRX8 layout)
11. **RDL passivation (1µm CVD Oxide / Nitride)**

    (Litho mask required-->not foreseen in TRX8 layout)

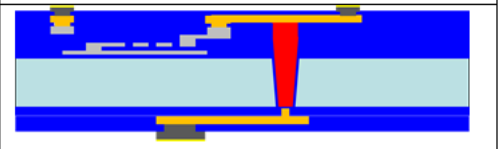


12. **Back side pad metallization deposited**

    (Litho mask required-->not foreseen in TRX8 layout)



13. **Temporary carrier de-bonding**



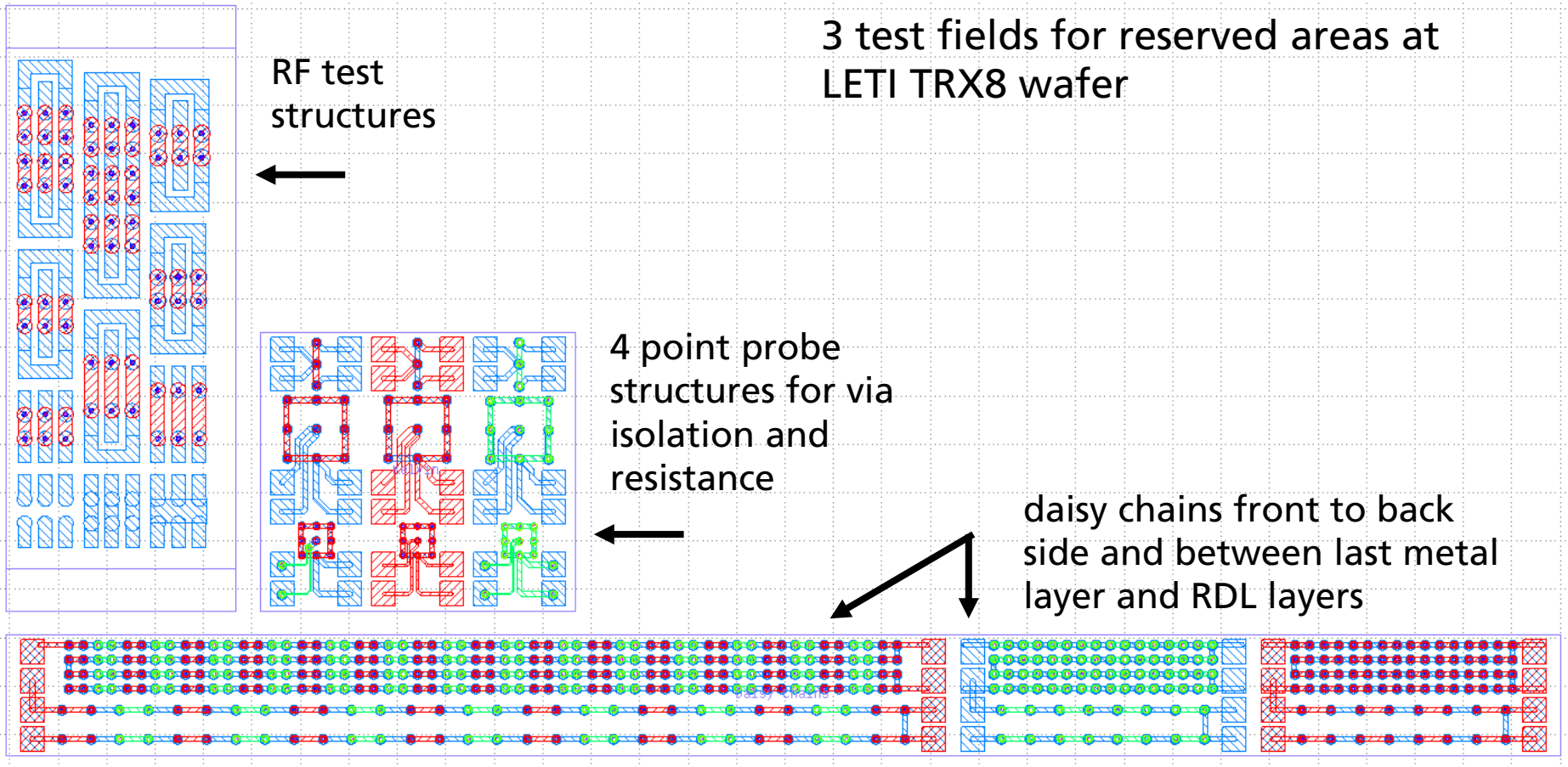
Layers and Test Structures for TSV Characterization

Frontside:

- #61 – top metal on LETI Wafe (line 20µm, pad Ø30µm)
- #10 – TSV (Ø20µm)
- #11 – FS-RDL metal (line 20µm, pad Ø40µm)

Backside:

- #09 – BS TSV-passopen (via Ø10µm)
- #21 – BS-RDL metal (line 20µm, pad Ø30µm)



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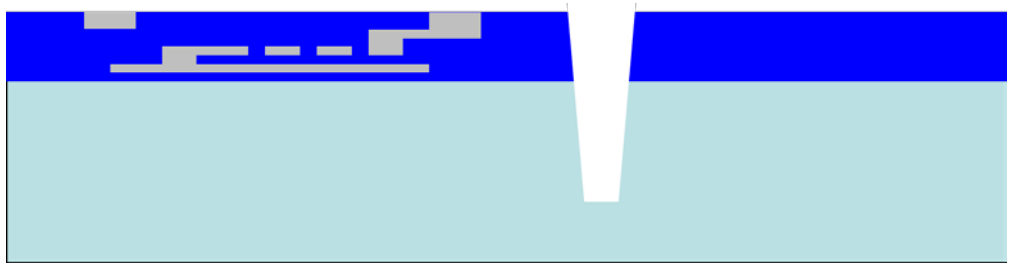
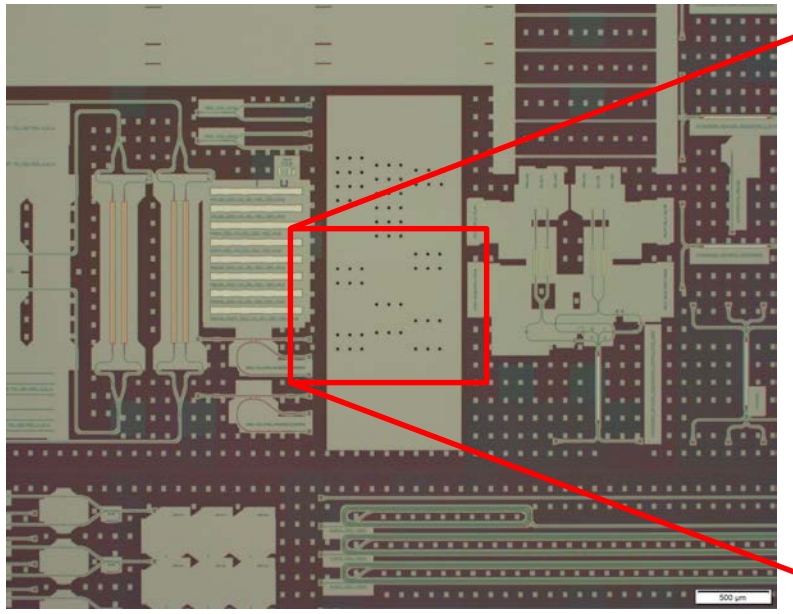
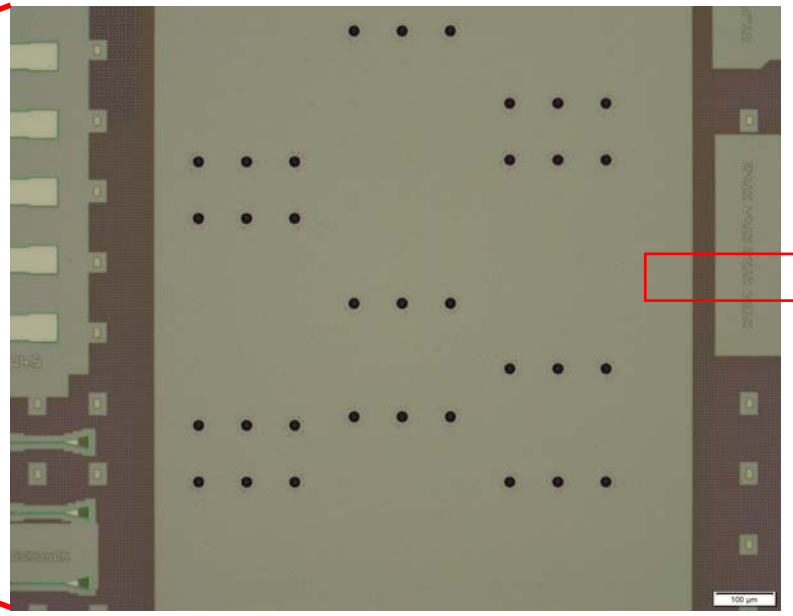
Wafer after TSV blind hole etching



- Lithography and Alignment established ✓
- BEOL etching established ✓
- SI-DRIE etching established ✓
- CVD / PVD / Cu-Plating to be done





Acknowledgement

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MASSTART project is an initiative of the **Photonics Public Private Partnership** www.photonics21.org

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