Develop your custom Photonic Integrated Circuit for Data Centers

Dr. Katarzyna ŁAWNICZUK
VP, Bright Photonics BV, Netherlands

virtual conference session:
Data Center Interconnects – Towards Mass Manufacturing
online / October 6th 2020 / 4 – 7pm

Develop your custom Photonic Integrated Circuit for Data Centers

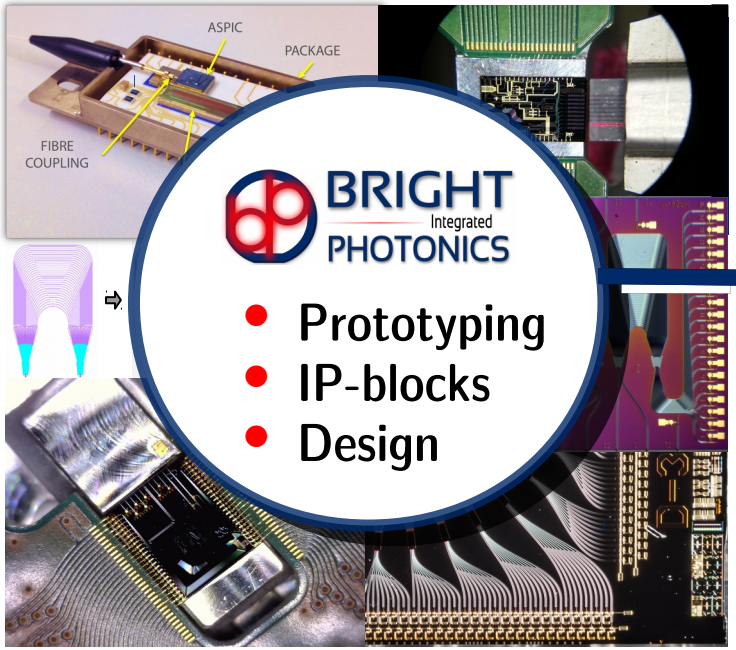
Technology selection and design & validation

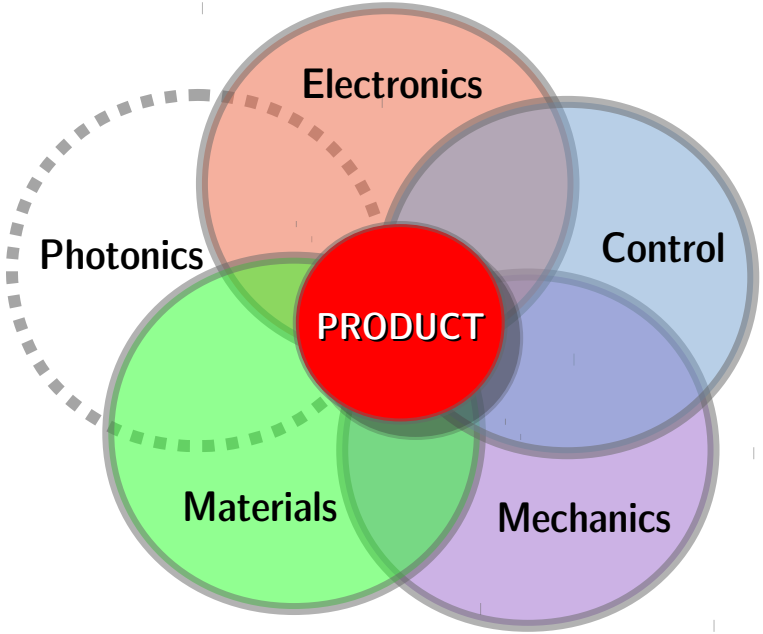
Katarzyna Ławniczuk
k.lawniczuk@brightphotonics.eu

Photonics Days 2020 – Berlin Brandenburg
6 October 2020

About BRIGHT Photonics:

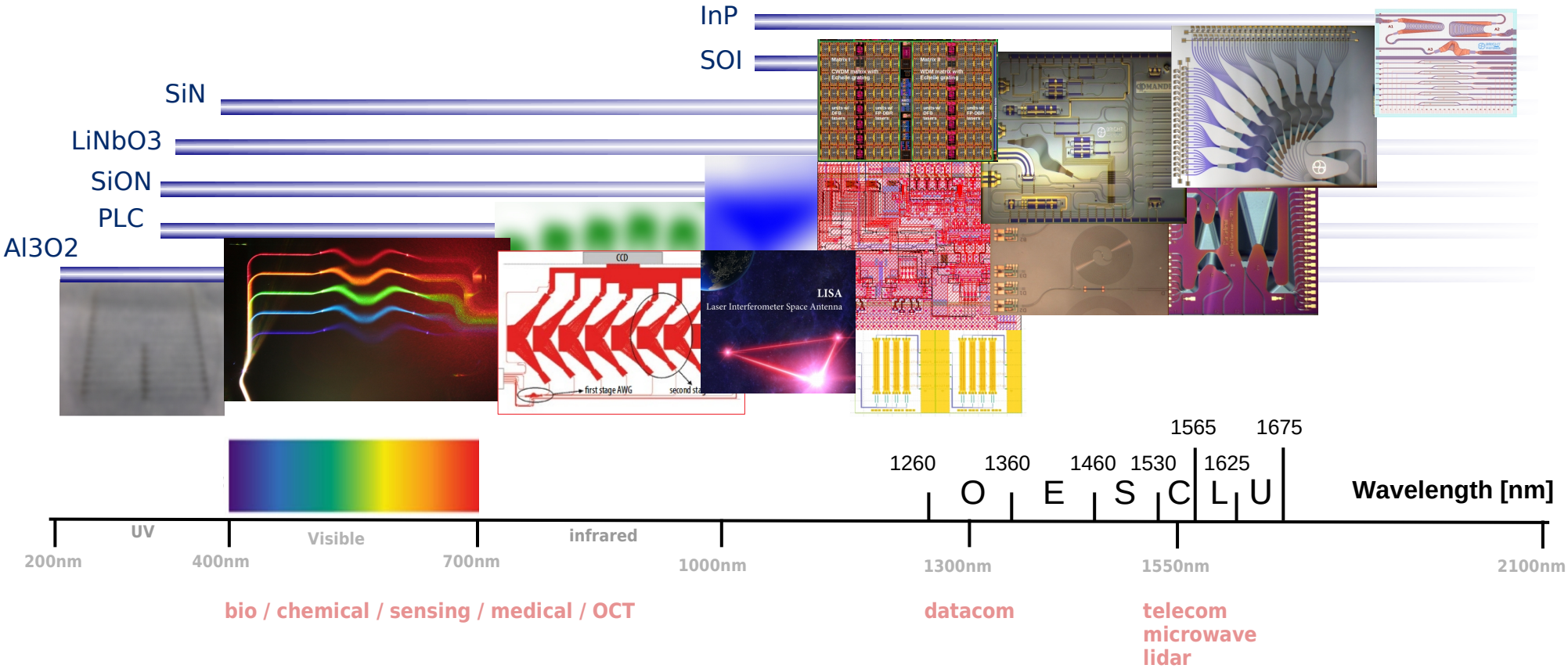
Empowering products with photonic engineering





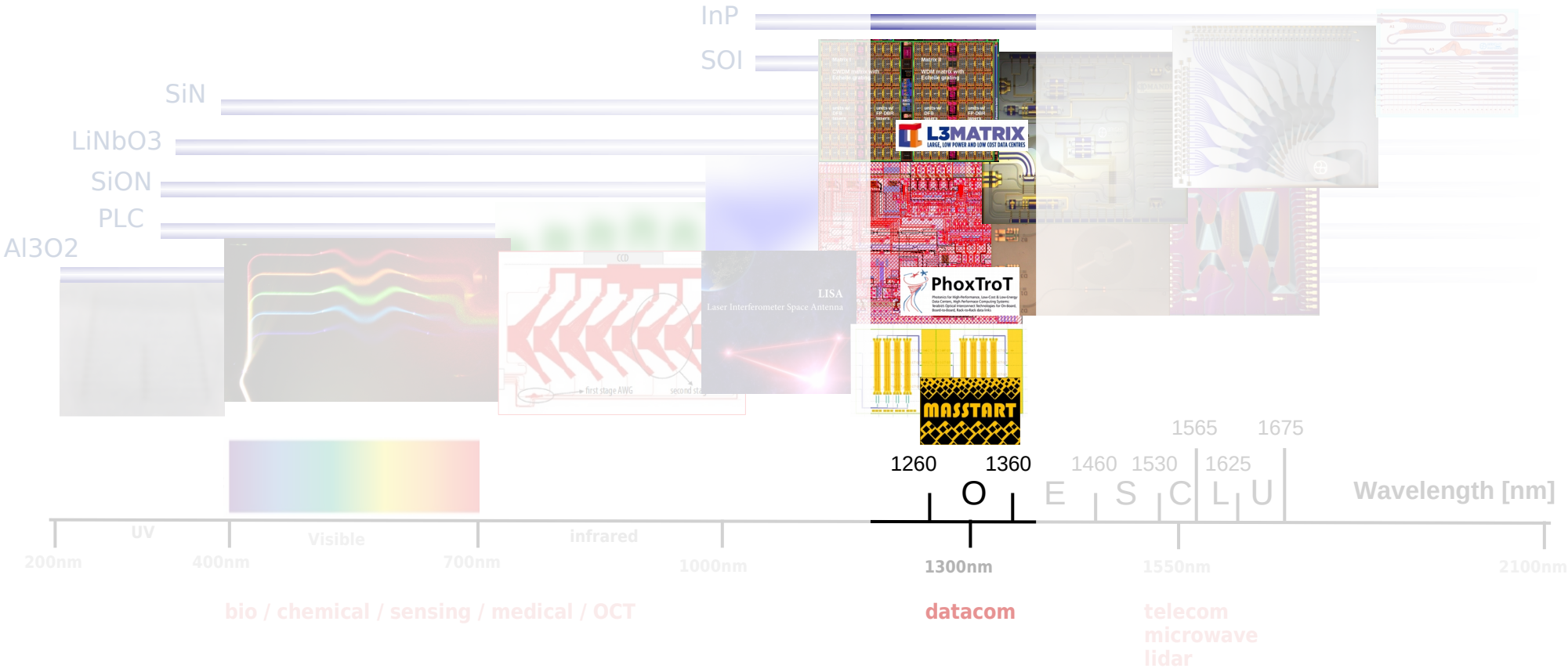
About BRIGHT Photonics:

Design across wavelengths from UV to IR



About BRIGHT Photonics:

Design across wavelengths from UV to IR



Development beyond 400G in EU projects

BRIGHT's contribution:

A. Design of optical interconnects
- chip-to-chip
- chip-to-board
- fiber-to-chip/board

B. IP blocks & PIC concepts
- mux/de-mux, couplers,
- lasers, Rx, Tx, switching PICs

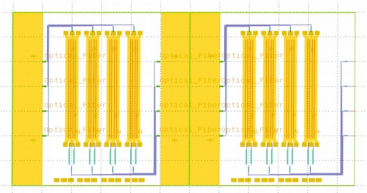
C. Integration of technologies

D. PIC layout design & validation tools

Nazca design™

1.6 Tb/s
16-ch. WDM

MASSTART

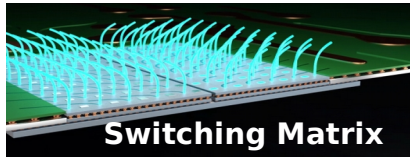


Transceivers for Tb/s inter and intra Data Centers applications

1.6 Tb/s
8x8 switching matrix

L3MATRIX
LARGE, LOW POWER AND LOW COST DATA CENTRES

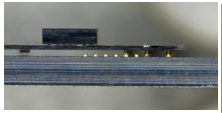
Co-Package Technology Platform

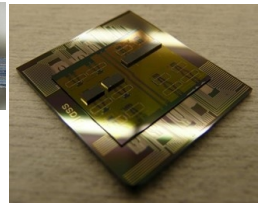


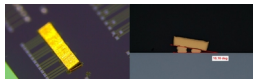
480 Gb/s
12 ch. Tx/Rx

PhoxTroT

Optical Interconnections & 3D Integration Technologies

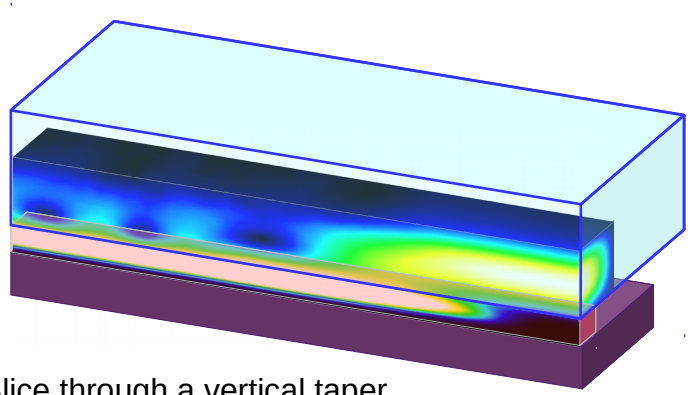




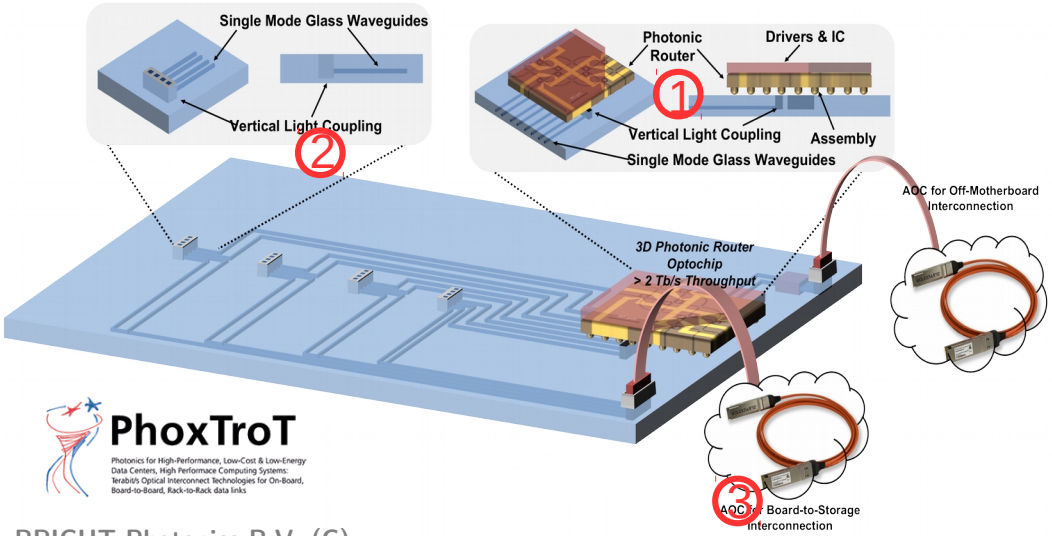


Funded by the European Union

A. Optical interconnects

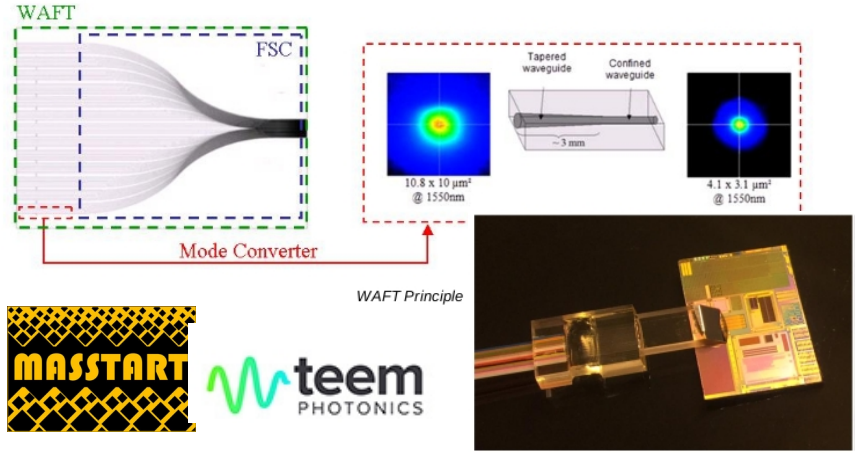


Slice through a vertical taper



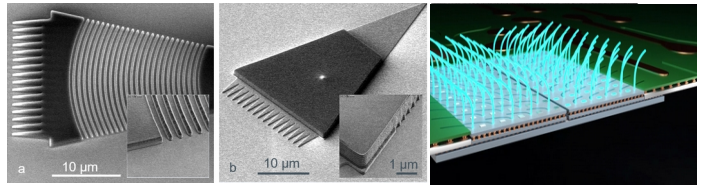
PhoxTroT

Photonics for High-Performance, Low-Cost & Low-Energy Data Centers, High Performance Computing Systems: Terabit/s Optical Interconnect Technologies for On-Board, Board-to-Board, Rack-to-Rack data links



MASSTART

teem PHOTONICS

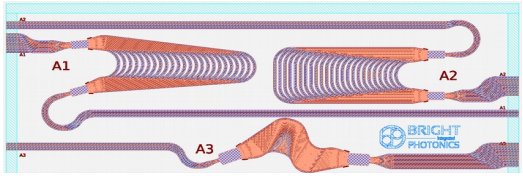


amu IBM L3MATRIX

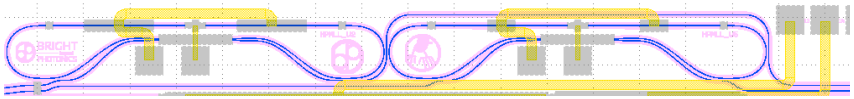
LARGE, LOW POWER AND LOW COST DATA CENTRES

B. IP-blocks and PIC concepts

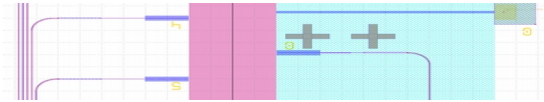
- Commercial MUX and DeMUX components



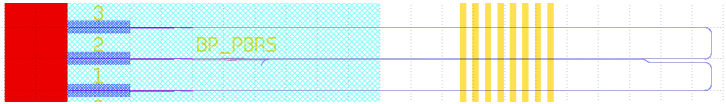
- Lasers (O-band, C-band)



- Spot-size converters

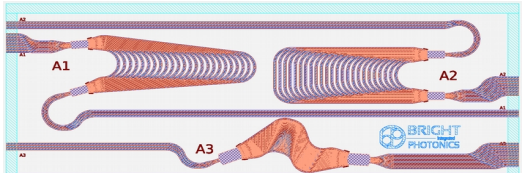


- Polarization handling devices

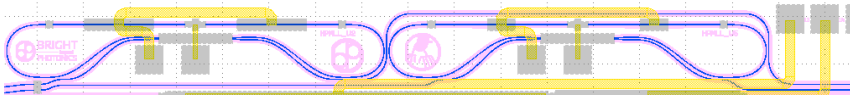


B. IP-blocks and PIC concepts

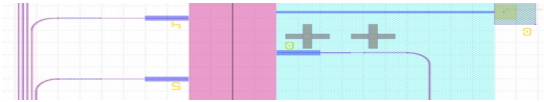
- Commercial MUX and DeMUX components



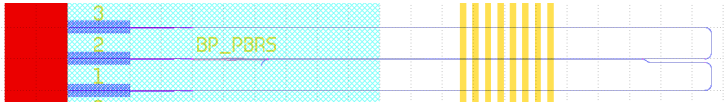
- Lasers (O-band, C-band)

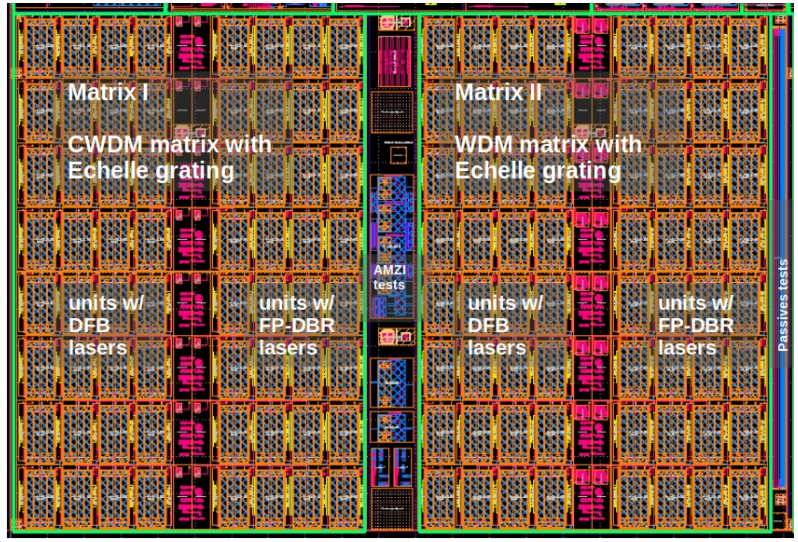


- Spot-size converters



- Polarization handling devices

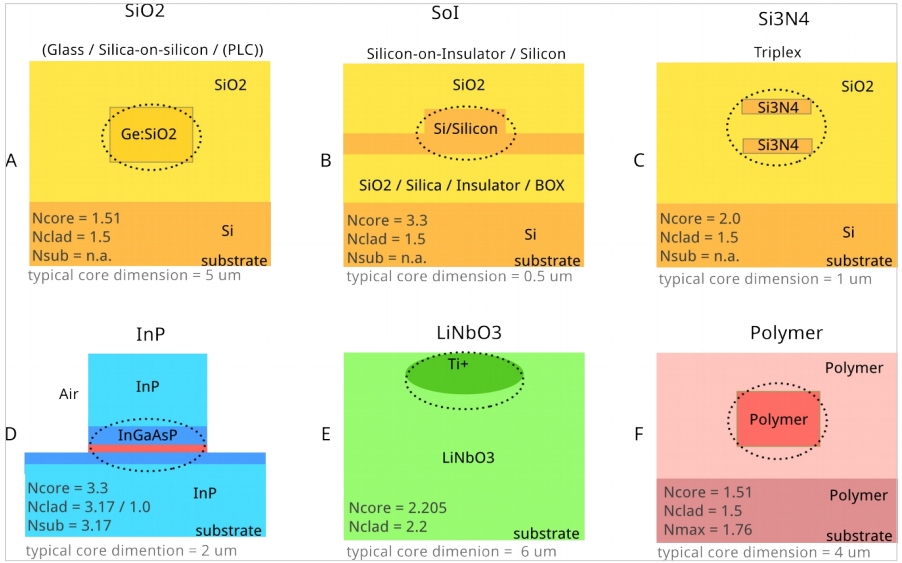




L3Matrix: switching matrix

C. Integration technologies: combining (low-loss) passives and actives

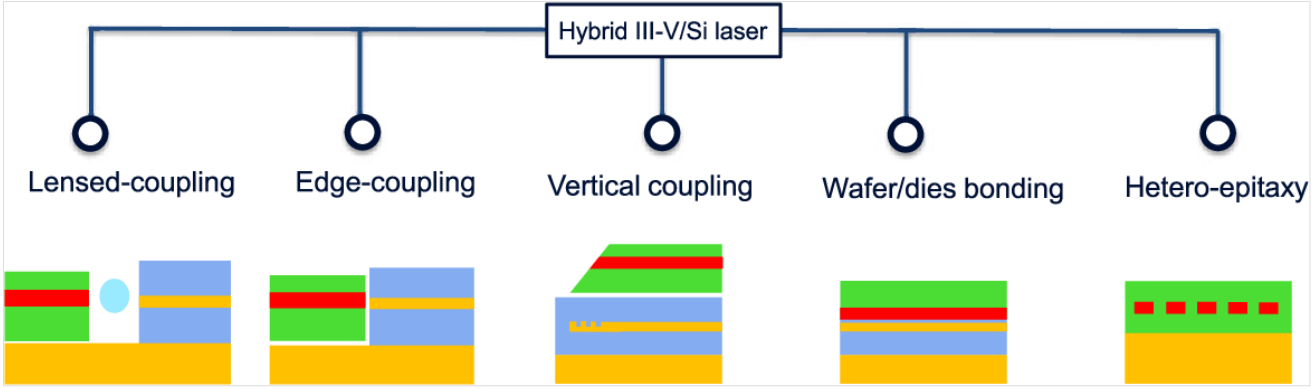
➔ monolithic vs. hybrid integration



Variety of material platforms

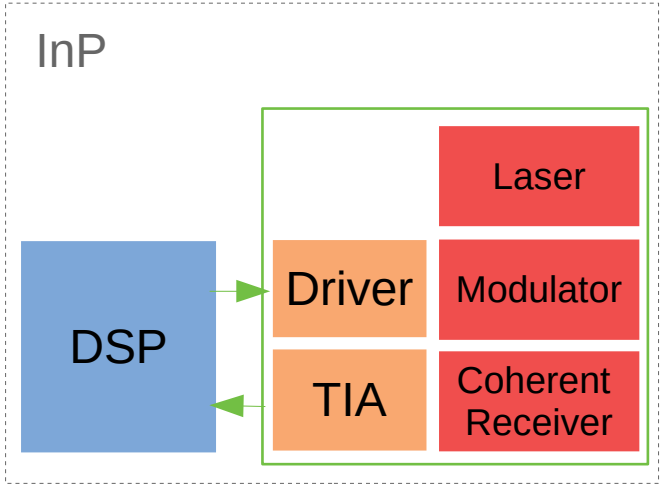
C. Integration technologies: combining (low-loss) passives and actives

- monolithic vs. hybrid integration
- hybrid III-V/Si laser integration



G. de Valicourt et al., JLT, 36 (2) 2018.

C. Integration technologies: Transceivers always combine InP and Si

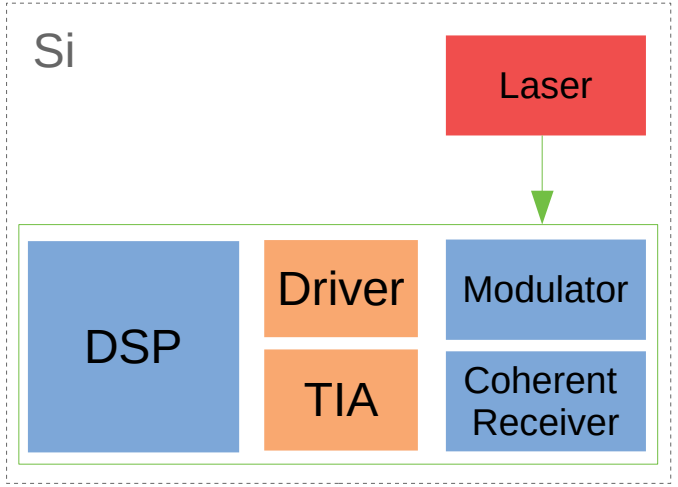


InP enables integration of everything except the DSP

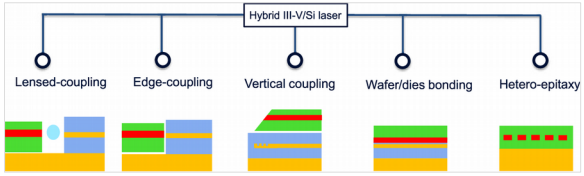
CMOS

SiGe

InP



Si enables integration of all electronic and photonic components except the laser



C. Integration technologies: comparison

		InP (generic integration)	SiP with external lasers	Heterogeneous integration (SOI)	Epitaxial growth on Si
Technical	Optical loss		0.1 dB LETI (rib)		
	Active/lasers coupling	0.1 dB butt-join	2-8 dB chip-to-chip	0.5 dB taper loss	0.1 dB butt-join
	Photodiodes				
	Mux/DeMUX				
	Polarization Control				
	Electronics integration				
Production	III-V substrate	✓	✓	✓	-
	III-V growth	✓	✓	✓	✓
	SOI/Si substrate	-	✓	✓	✓
	Footprint	High index contrast in 1D	High index contrast in 2D	High index contrast in 2D	High index contrast in 2D
	Yield		CMOS level		
Economic	Substrate cost ($/cm^2)	4.5	0.2	1.5	0.2
	Assembly costs	Fiber coupling	Laser coupling	III-V bonding	Fiber coupling
	Testing	Wafer level	Lasers, SiP	Wafer level	Wafer level
	Wafer size/scaling up	100 mm		300 mm	
Foundries / Product owners		Smart Photonics, Fraunhofer HHI / Infinera, Finisar	VTT, LETI, imec / Luxtera, Rockley	LETI, imec, TU/e - IMOS / Intel	Under research AIM, imec

C. Integration technologies: comparison

		InP (generic integration)	SiP with external lasers	Heterogeneous integration (SOI)	Epitaxial growth on Si
Technical	Optical loss		0.1 dB LETI (rib)		
	Active/lasers coupling	0.1 dB butt-join	2-8 dB chip-to-chip	0.5 dB taper loss	0.1 dB butt-join
	Photodiodes				
	Mux/DeMUX				
	Polarization Cont				
	Electronics integ				
Production	III-V substrate			✓	-
	III-V growth			✓	✓
	SOI/Si substrate			✓	✓
	Footprint			h index contrast in 2D	High index contrast in 2D
	Yield			CMOS level	
Economic	Substrate cost ($/cm²)	4.5	0.2	1.5	0.2
	Assembly costs	Fiber coupling	Laser coupling	III-V bonding	Fiber coupling
	Testing	Wafer level	Lasers, SiP	Wafer level	Wafer level
	Wafer size/scaling up	100 mm		300 mm	
Foundries / Product owners		Smart Photonics, Fraunhofer HHI / Infinera, Finisar	VTT, LETI, imec / Luxtera, Rockley	LETI, imec, TU/e - IMOS / Intel	Under research AIM, imec

- → **Application / Spec**
- → **Volume**
- → **Yield**
- → **Cost**

C. Integration technologies: Moving towards complex modular systems

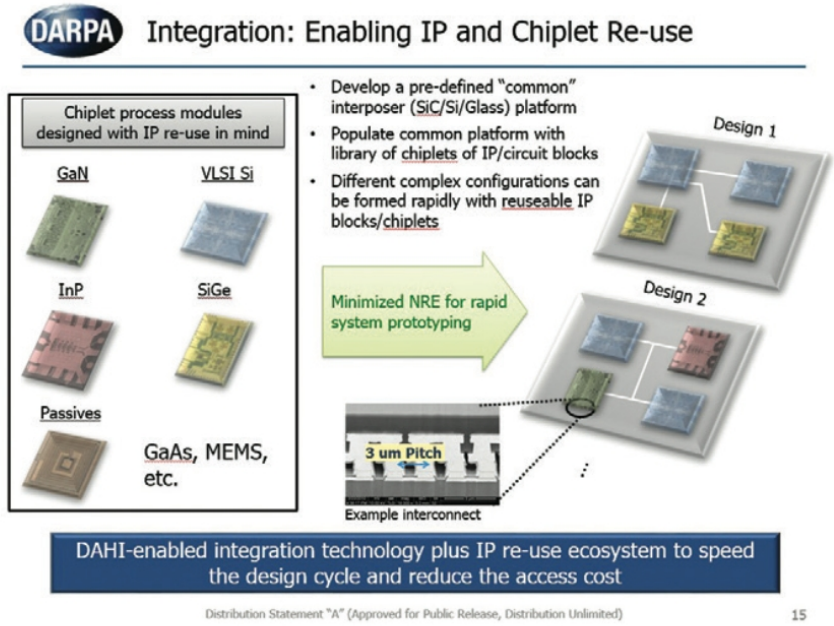


FIGURE 2. A key feature of CHIPS is the establishment of standard interfaces to promote the reusability and inter-changeability of modular circuit functional blocks or chiplets.

Beyond 50000G?

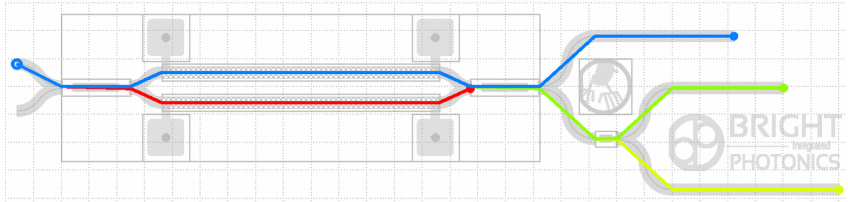
50 GHz bandwidth
x 2 symbols per period
x 4 bits per symbol (16QAM)
x 8 lanes
x 8 wavelengths
x 2 polarizations

= 51.2 Tb/s

D. Design and validation with Nazca-Design

Nazca design™
photonic IC design framework

- ✓ **Combine** multiple technologies – Hybrid design
  - ➔ Si-Photonics, III-V, Glass
  - ➔ Develop PDK, define and separate technology layers: layers mapping
- ✓ **Exchange** IP Building Blocks – IP protection
  - ➔ Combine files and create libraries with GDS BBs, cells mapping
  - ➔ IP BBs handling, work with GDSII standard
  - ➔ Facilitated GDSII files scaling and proper accuracy
- ✓ **Solve** complex routing and DRC
  - ➔ Create interconnects and routing for circuits connectivity with error-free implementation & DRC on connectivity
  - ➔ Path tracing for circuit integrity
- ✓ **Facilitate** new generation of assembly, coupling and packaging approaches
  - ➔ Create packaging rules, packaging templates,
  - ➔ Import fiducials, drivers, tias

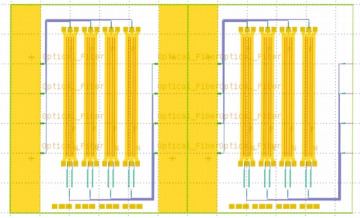



```
# import PDK
# import IP BBs
# import Packages

import nazca
import leti
import teem
import izm
import ficontec
import bright
```

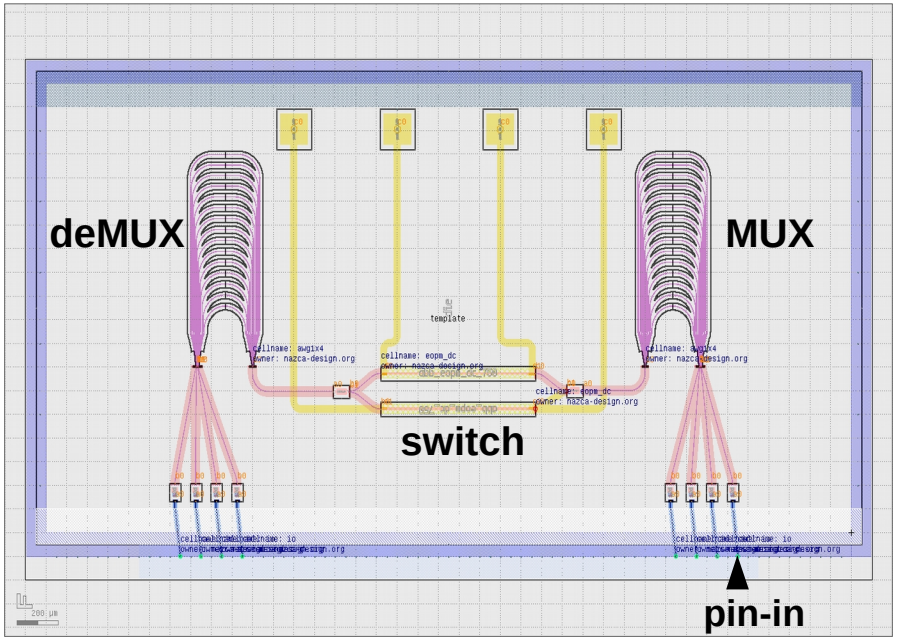
MASSTART

Mellanox
ADVA Optical Networking



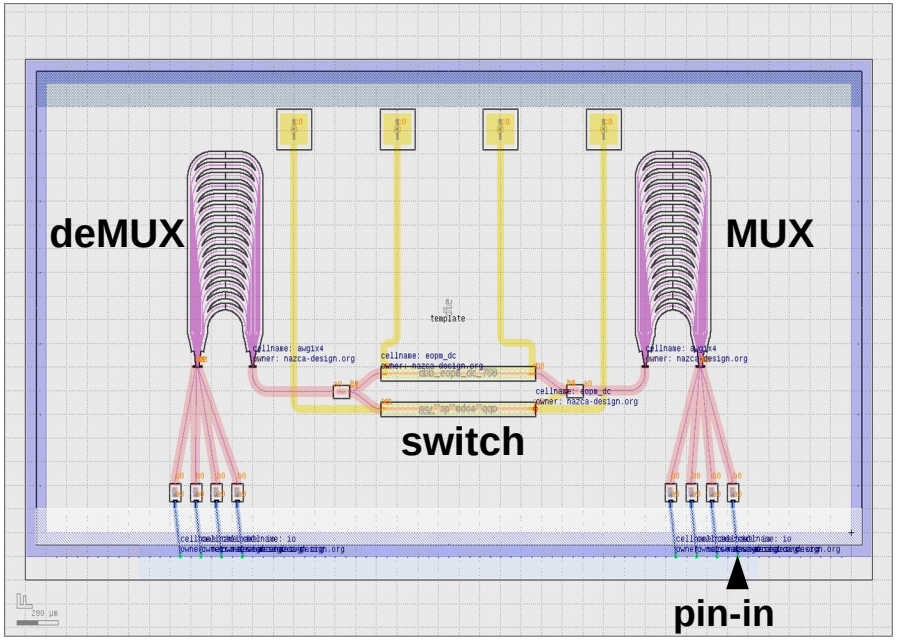
Data Center applications

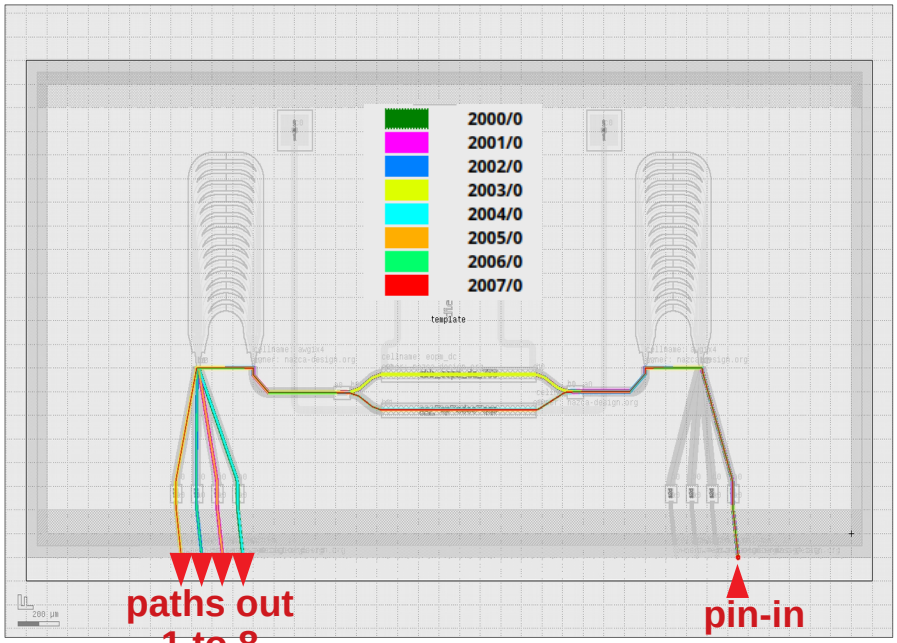
D. Design and validation in GDS



Nazca design™
photonic IC design framework

D. Design and validation in GDS: path tracing

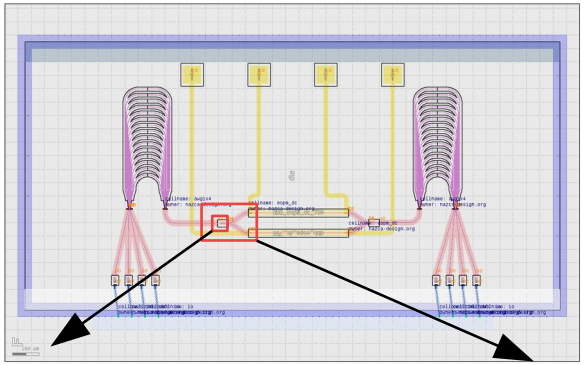




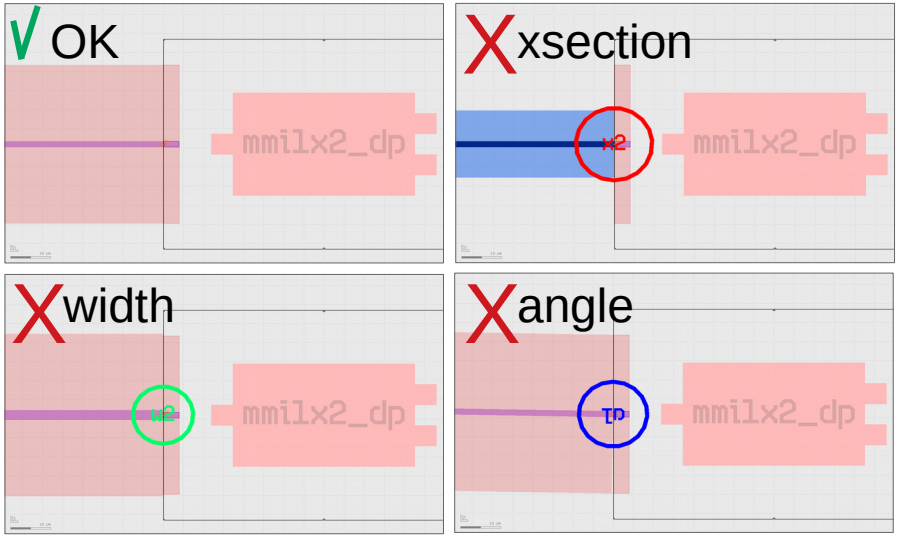
Nazca design™
photonic IC design framework

D. Design and validation in GDS: connection DRC

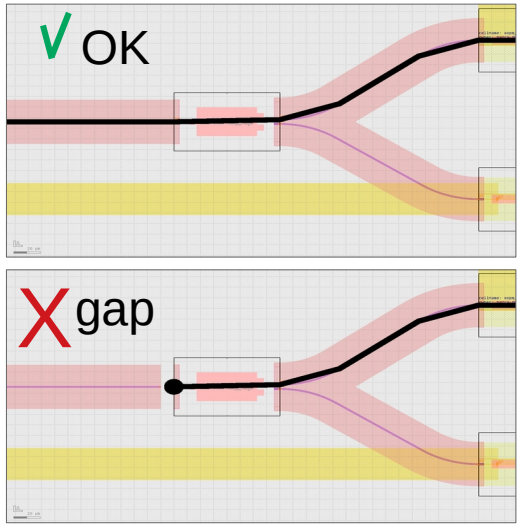
Nazca design™
photonic IC design framework



pin2pin



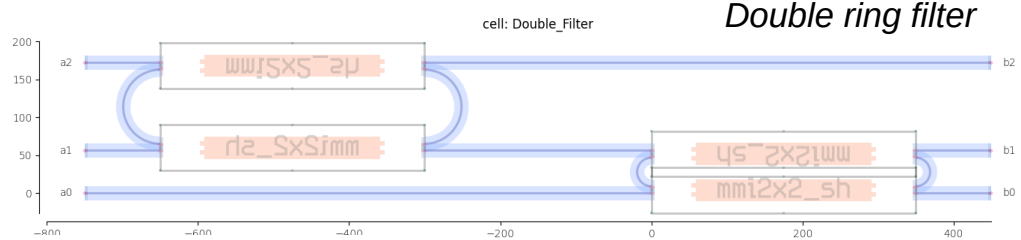
path

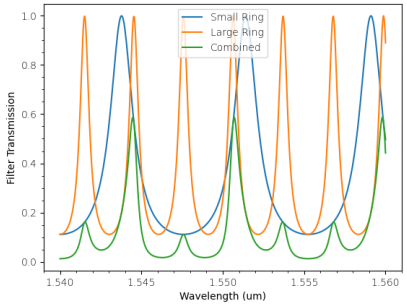


D. Design and validation in GDS: circuit simulation and verification at GDS level

Nazca design™
photonic IC design framework

Double ring filter

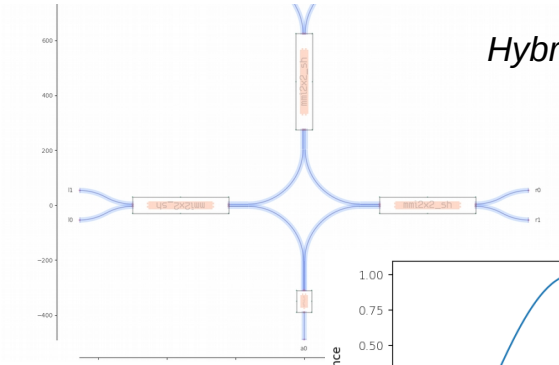


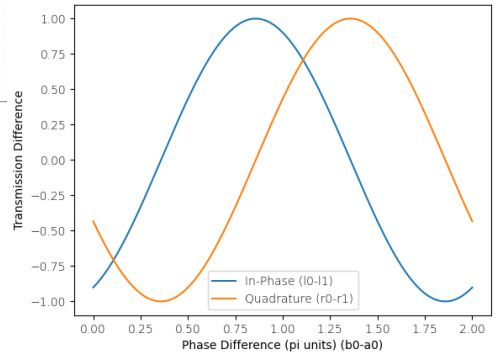


Examples:
- Investigation of filtering characteristics
- Transmission simulation of a circuit
- Integration of Material models in PDK and components S-matrices

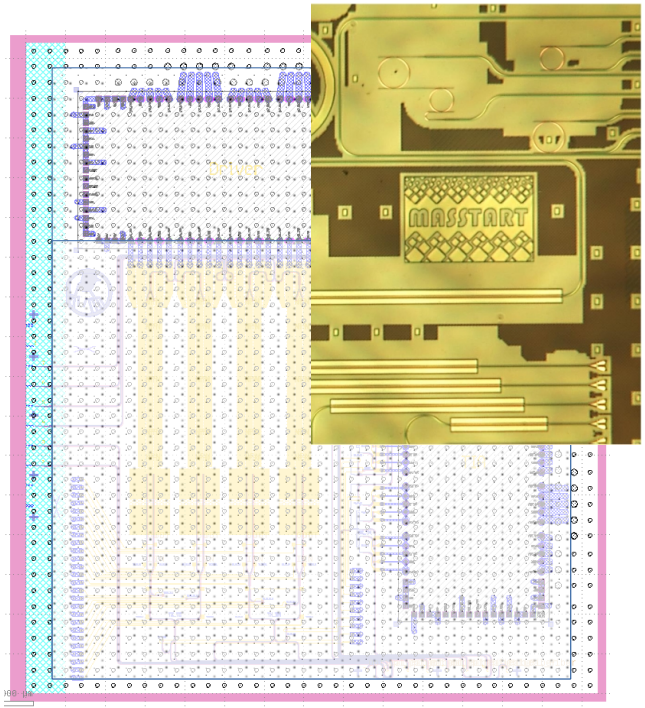
www.nazca-design.org

Hybrid - 90

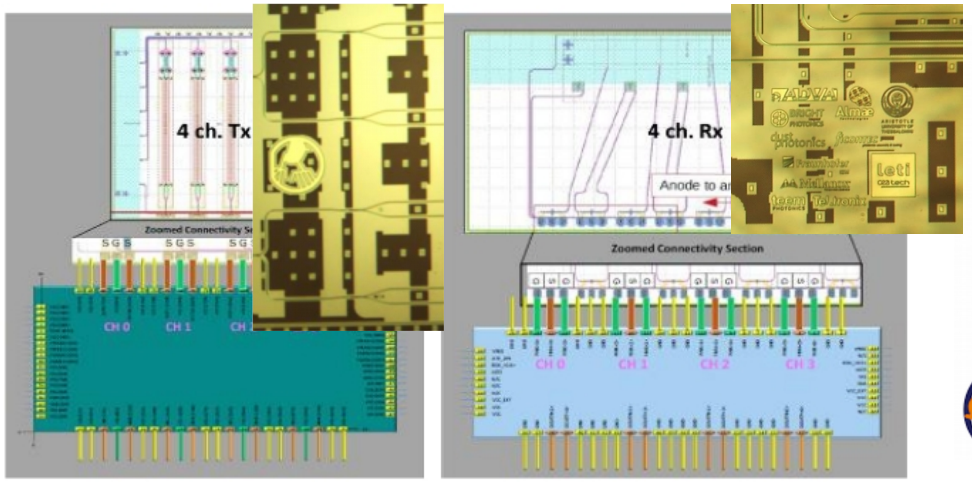




D. Design and validation with Nazca-Design



Tape-out of MASSTART inter- and intra- Data Center PICs



Nazca design™
photonic IC design framework

Thank you!

Contact: info@BrightPhotonics.eu

- ✔ Supply chain development
- ✔ PIC concepts & IP blocks
- ✔ Prototyping & Design

MASSTART team:
Marco Passoni
Katarzyna Ławniczuk
Ronald Broeke

Acknowledgement

Co-funded by the Horizon 2020
Framework Programme of the European Union

MASSTART project is co-funded by the Horizon 2020 Framework Programme of the European Union with Grant Agreement Nr. 825109. https://cordis.europa.eu/project/rcn/219912/factsheet/en

MASSTART project is an initiative of the **Photonics Public Private Partnership** www.photonics21.org

#Photonics
@Photonics21
@PhotonicsEU
#H2020

PHOTONICS PUBLIC PRIVATE PARTNERSHIP

www.masstart.eu

#MASSTART