Develop your custom Photonic Integrated Circuit for Data Centers

Technology selection and design & validation

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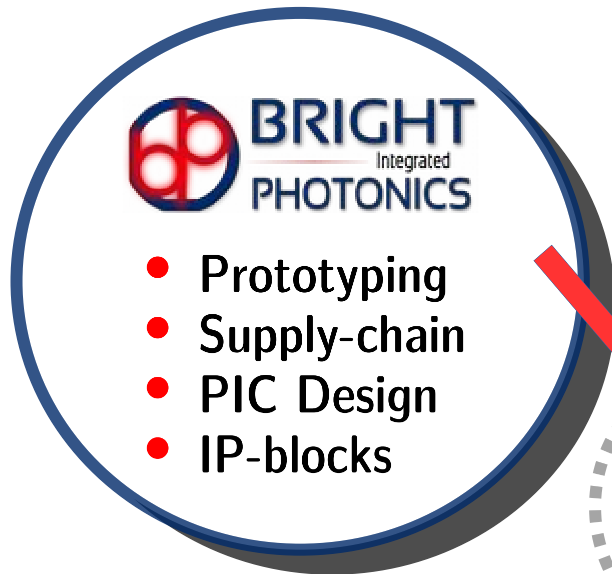
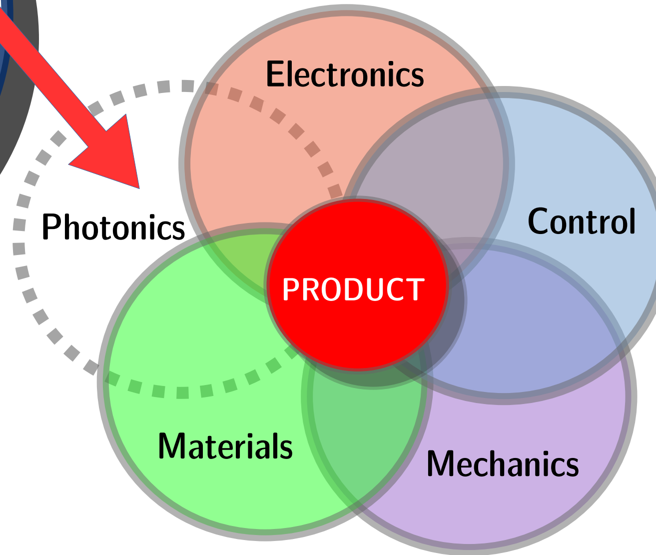
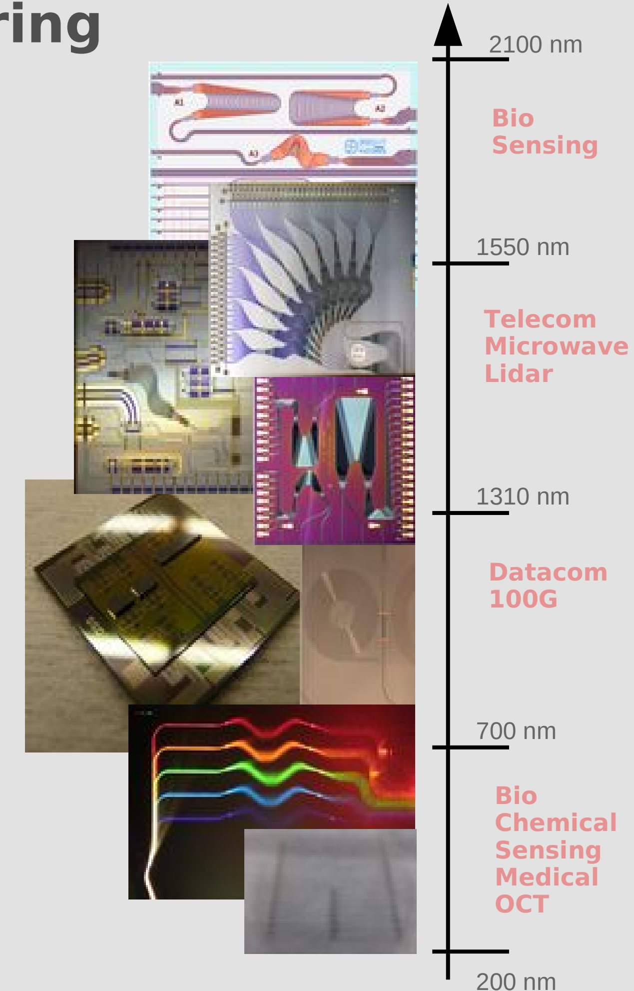
5 October 2021

Empower products with photonic engineering

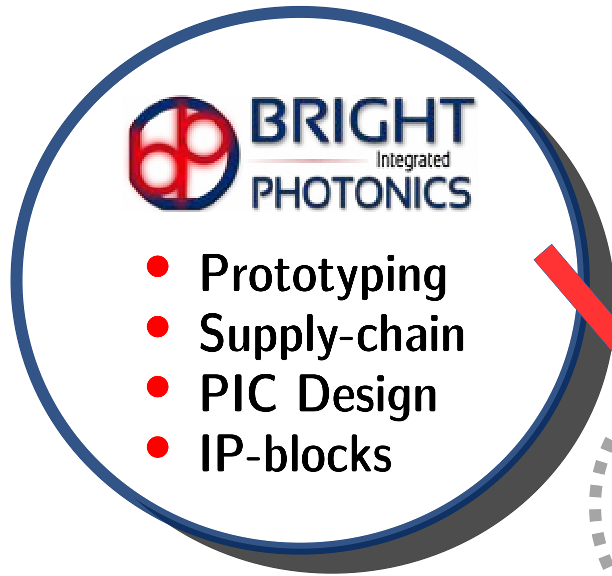


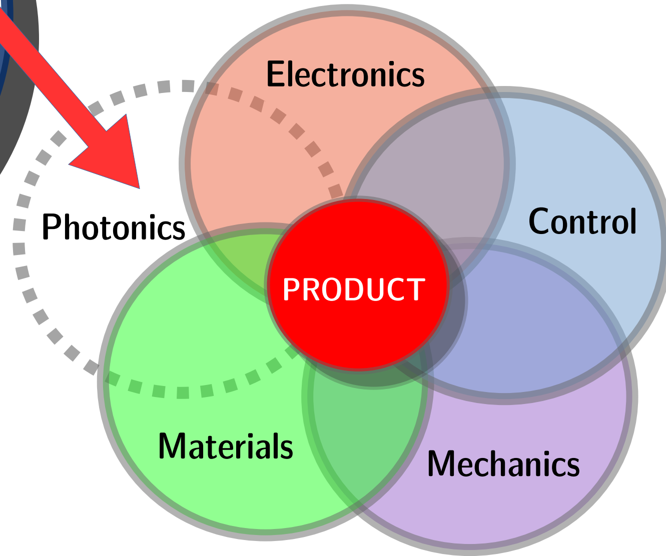


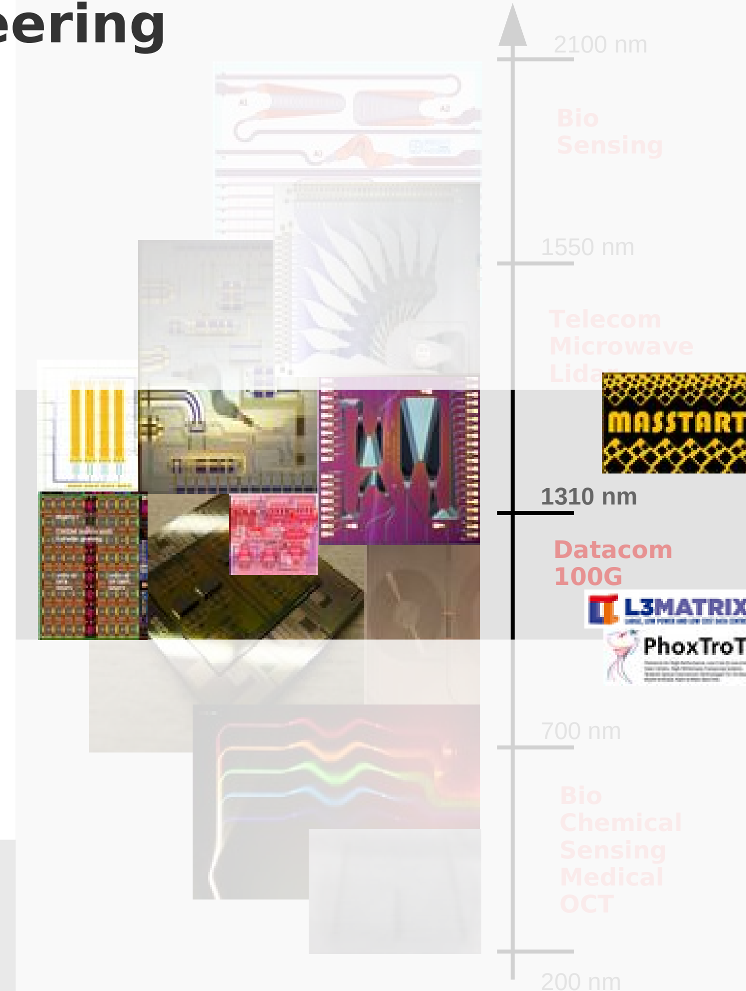


- ✔ **Design from UV to IR**
- ✔ **Design across technologies**
- ✔ **Design flow innovation**

Empower products with photonic engineering







- ✔ **Design from UV to IR**
- ✔ **Design across technologies**
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MASSTART: Exploitation scheme

MASS manufacturing of Transceivers for Terabit/s era

ADVA Optical Networking
Mellanox TECHNOLOGIES
dust photonics

System provider
Application user

BRIGHT Integrated PHOTONICS
Fraunhofer IZM

Design house &
technology consultancy

leti ceatech
teem PHOTONICS
Fraunhofer IZM
Almae
ficonTEC photonics assembly & testing

Technology &
equipment providers

BRIGHT Photonics B.V. (C)

Development beyond 400G in EU projects

BRIGHT's contribution:

A. Design of optical interconnects
   - chip-to-chip
   - chip-to-board
   - fiber-to-chip/board

B. IP blocks & PIC concepts
   - mux/de-mux, couplers, lasers, Rx, Tx, switching PICs

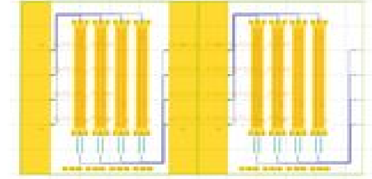
C. Integration of technologies

D. PIC layout design & validation tools; PDK

480 Gb/s
12 ch. Tx/Rx

1.6 Tb/s
8x8 switching matrix

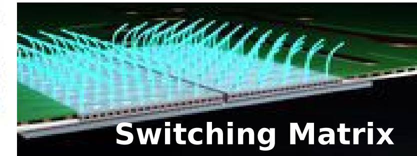
1.6 Tb/s
16-ch. WDM

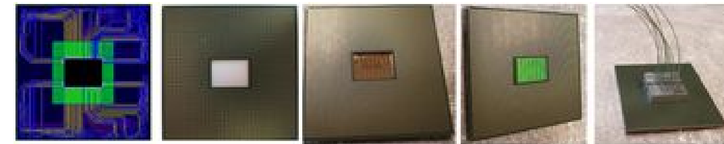


Transceivers for Tb/s inter and intra Data Centers applications

L3MATRIX
LARGE, LOW POWER AND LOW COST DATA CENTRES

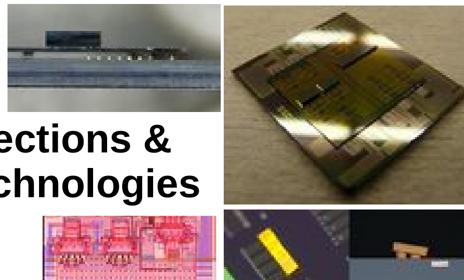
Co-Package Technology Platform





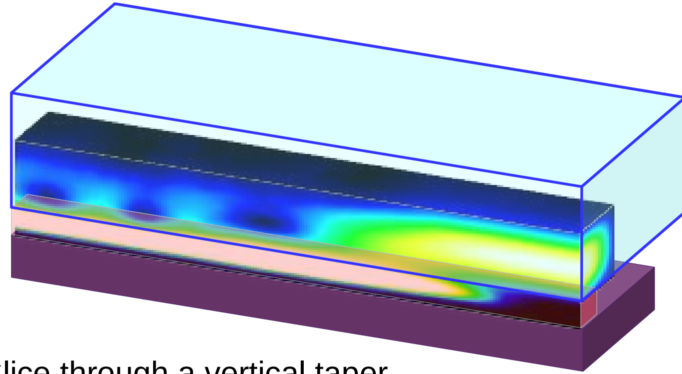
PhoxTroT

Optical Interconnections & 3D Integration Technologies

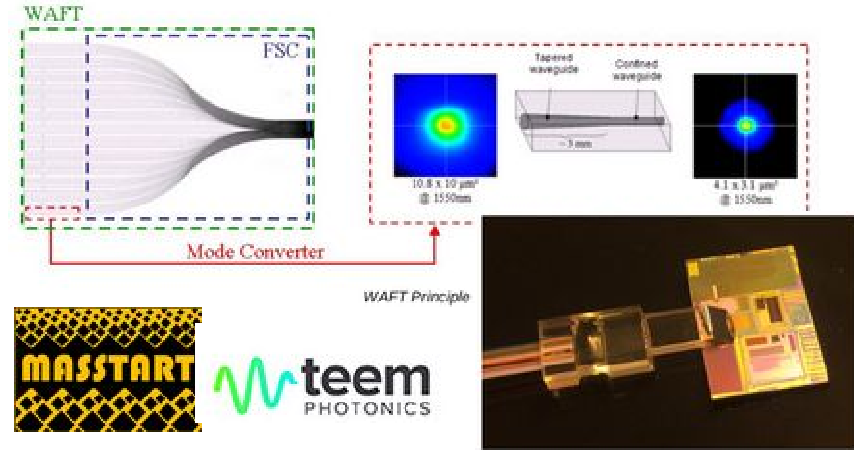


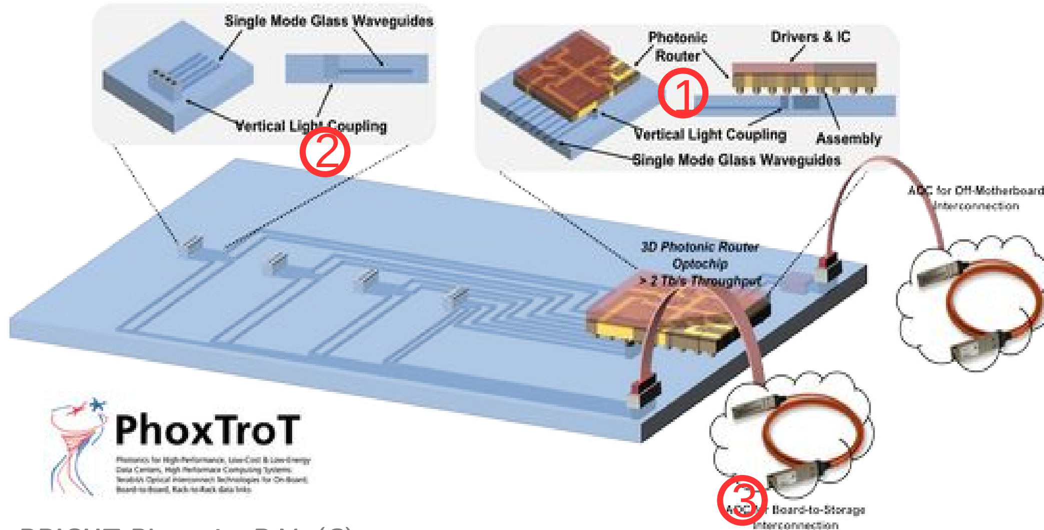
Funded by the European Union

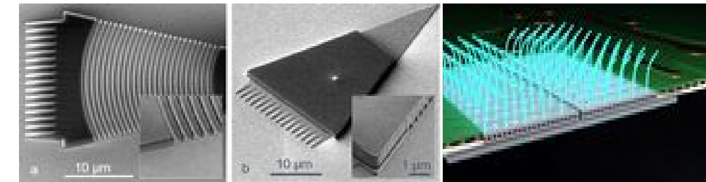
A. Optical interconnects

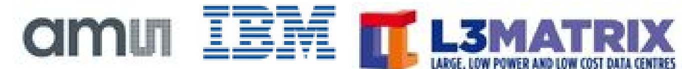


Slice through a vertical taper







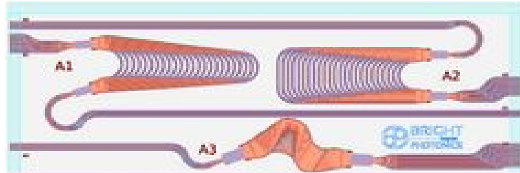


B. IP-blocks and PIC concepts

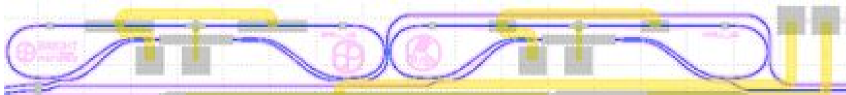
Your ‘custom’ optical engines

BRIGHT Integrated PHOTONICS

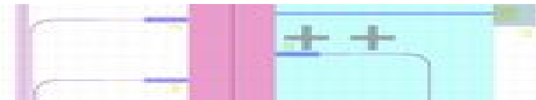
- Commercial MUX and DeMUX components



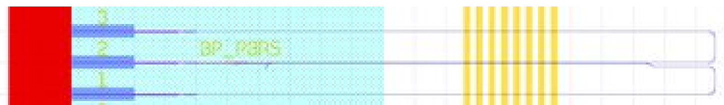
- Lasers (O-band, C-band)



- Spot-size converters



- Polarization handling devices



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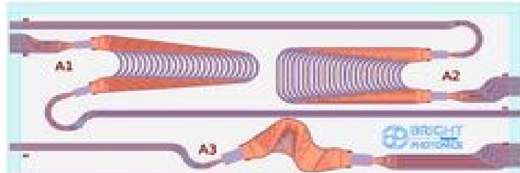

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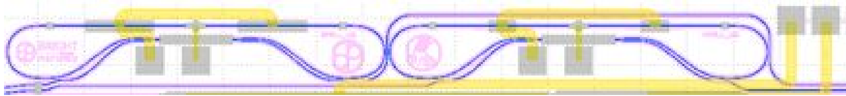

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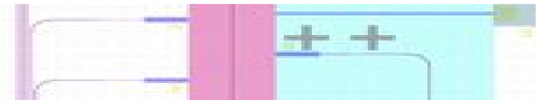

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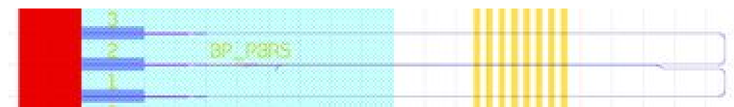
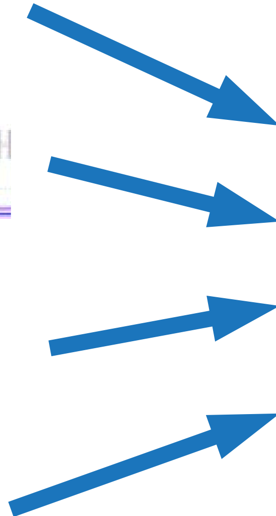
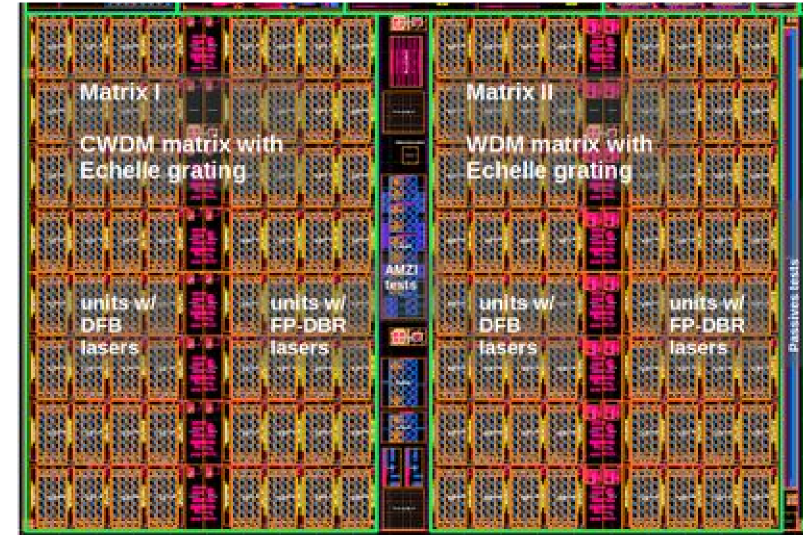


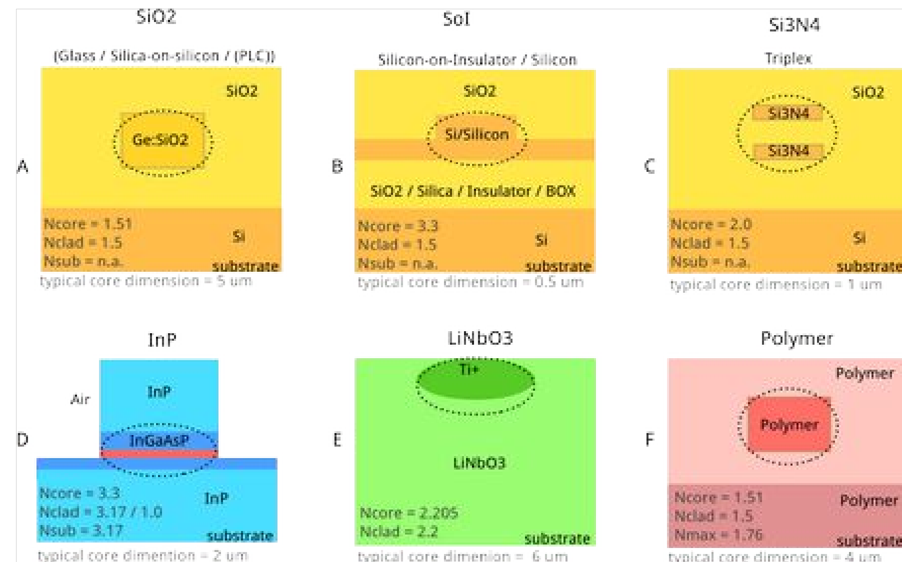




L3Matrix: switching matrix

C. Integration technologies: combining (low-loss) passives and actives

➔ monolithic vs. hybrid integration

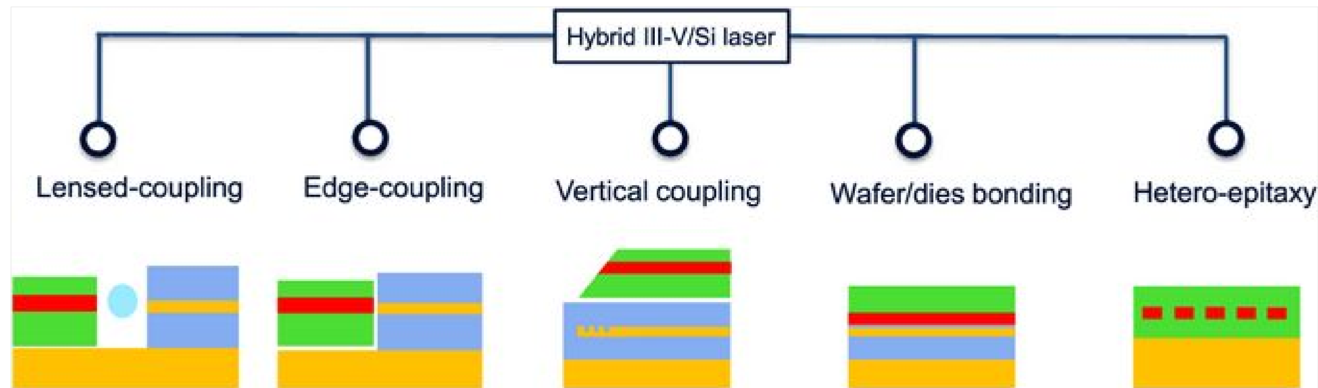


Variety of material platforms

C. Integration technologies: combining (low-loss) passives and actives

➔ monolithic vs. hybrid integration

➔ hybrid III-V/Si laser integration



G. de Valicourt et al., JLT, 36 (2) 2018.

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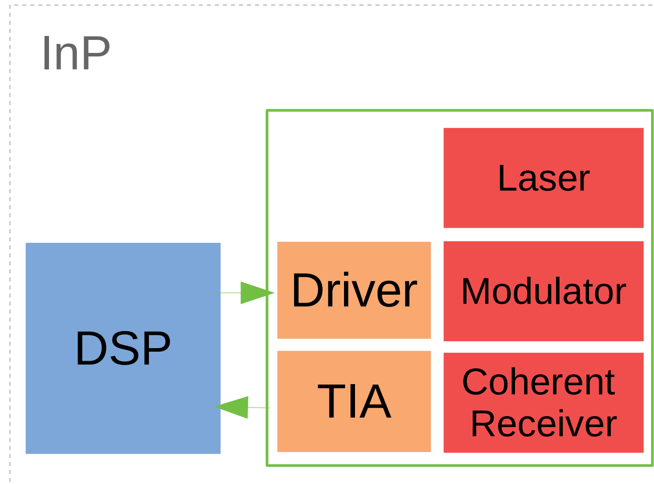
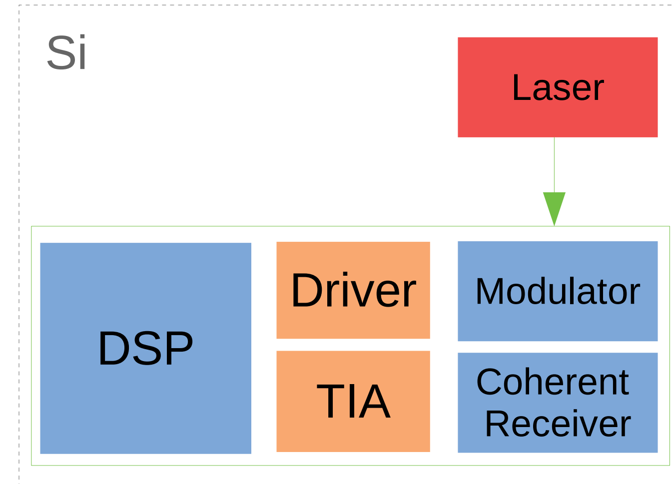
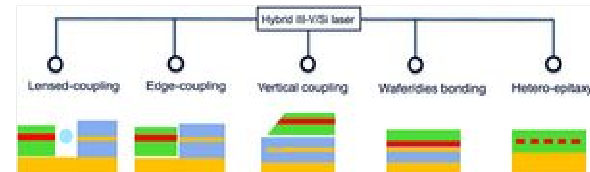
C. Integration technologies: Transceivers always combine InP and Si



InP enables integration of everything except the DSP



Si enables integration of all electronic and photonic components except the laser



C. Integration technologies: comparison

		InP (generic integration)	SiP with external lasers	Heterogeneous integration (SOI)	Epitaxial growth on Si
Technical	Optical loss		0.1 dB LETI (rib)		
	Active/lasers coupling	0.1 dB butt-join	2-8 dB chip-to-chip	0.5 dB taper loss	0.1 dB butt-join
	Photodiodes				
	Mux/DeMUX				
	Polarization Control				
	Electronics integration				
Production	III-V substrate	✓	✓	✓	-
	III-V growth	✓	✓	✓	✓
	SOI/Si substrate	-	✓	✓	✓
	Footprint	High index contrast in 1D	High index contrast in 2D	High index contrast in 2D	High index contrast in 2D
	Yield		CMOS level		
Economic	Substrate cost ($/cm^2)	4.5	0.2	1.5	0.2
	Assembly costs	Fiber coupling	Laser coupling	III-V bonding	Fiber coupling
	Testing	Wafer level	Lasers, SiP	Wafer level	Wafer level
	Wafer size/scaling up	100 mm		300 mm	
Foundries / Product owners		Smart Photonics, Fraunhofer HHI / Infinera, Finisar	VTT, LETI, imec / Luxtera, Rockley	LETI, imec, TU/e - IMOS / Intel	Under research AIM, imec

BRIGHT Integrated PHOTONICS

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➔ Application / Spec
➔ Volume
➔ Yield
➔ Cost

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C. Integration technologies: Moving towards complex modular systems

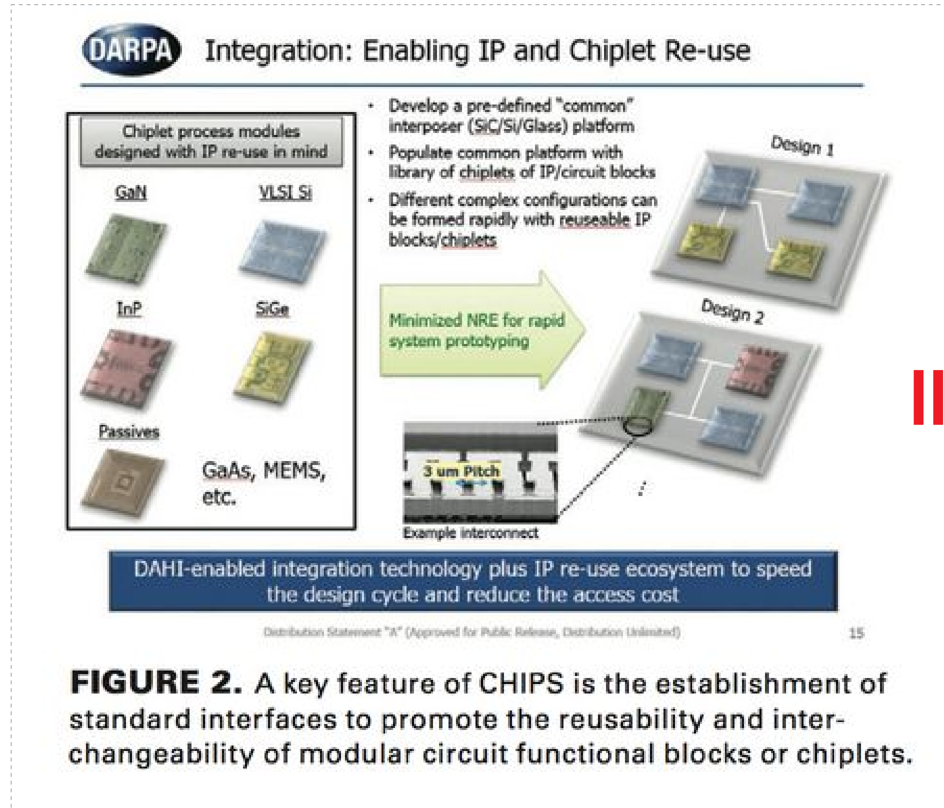

FIGURE 2. A key feature of CHIPS is the establishment of standard interfaces to promote the reusability and interchangeability of modular circuit functional blocks or chiplets.

Beyond 50000G?

50 GHz bandwidth
x 2 symbols per period
x 4 bits per symbol (16QAM)
x 8 lanes
x 8 wavelengths
x 2 polarizations

= 51.2 Tb/s

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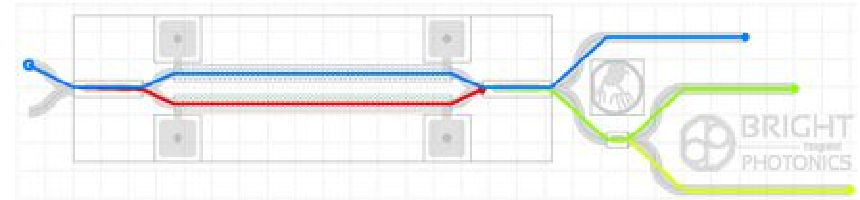
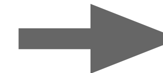
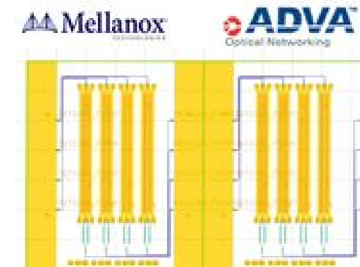
D. Design and validation with Nazca-Design

- ✓ **Combine** multiple technologies – Hybrid design
  - ➔ Si-Photonics, III-V, Glass
  - ➔ Develop PDK, define and separate technology layers: layers mapping
- ✓ **Exchange** IP Building Blocks – IP protection
  - ➔ Combine files and create libraries with GDS BBs, cells mapping
  - ➔ IP BBs handling, work with GDSII standard
  - ➔ Facilitated GDSII files scaling and proper accuracy
- ✓ **Solve** complex routing and DRC
  - ➔ Create interconnects and routing for circuits connectivity with error-free implementation & DRC on connectivity
  - ➔ Path tracing for circuit integrity
- ✓ **Facilitate** new generation of assembly, coupling and packaging approaches
  - ➔ Create packaging rules, packaging templates,
  - ➔ Import fiducials, drivers, tias



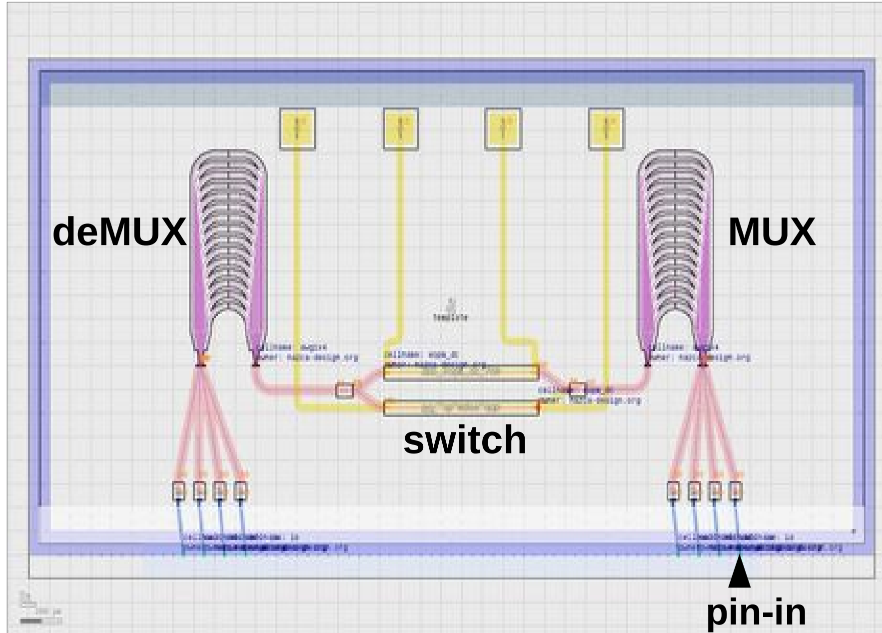

```
# import PDK
# import IP BBs
# import Packages

import nazca
import leti
import teem
import izm
import ficontec
import bright
```



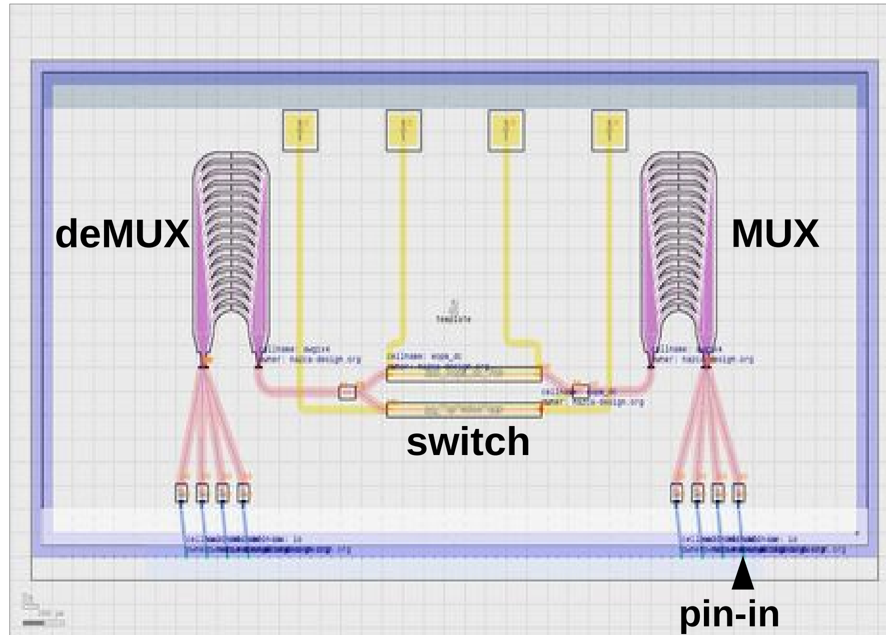


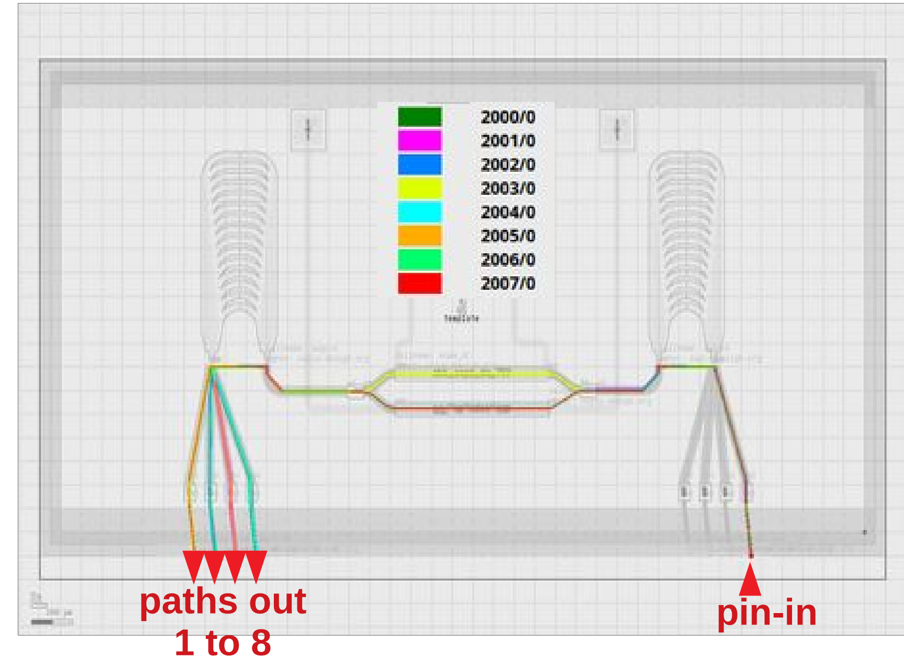
Data Center applications

D. Design and validation in GDS



D. Design and validation in GDS: path tracing





Nazca design™
photonic IC design framework

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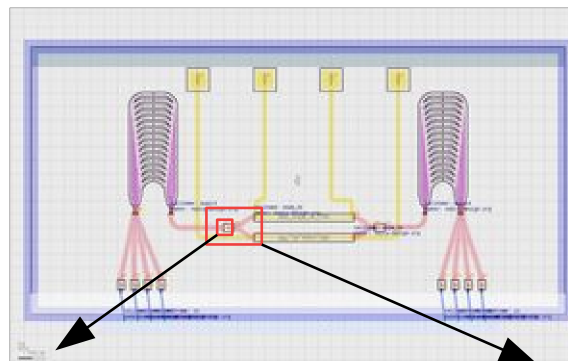
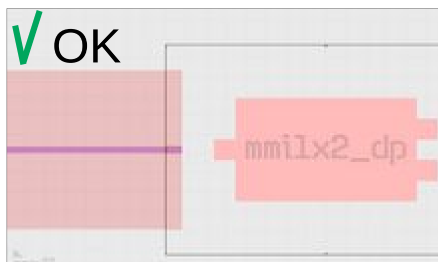
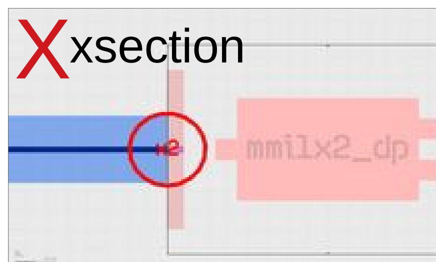
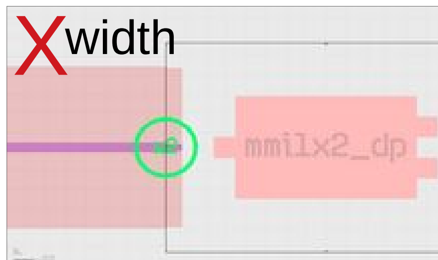
D. Design and validation in GDS: connection DRC

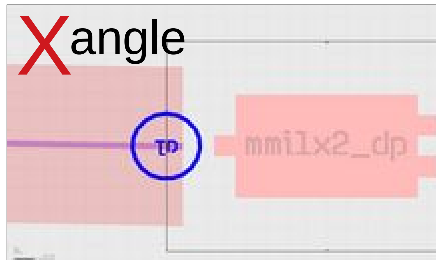


pin2pin

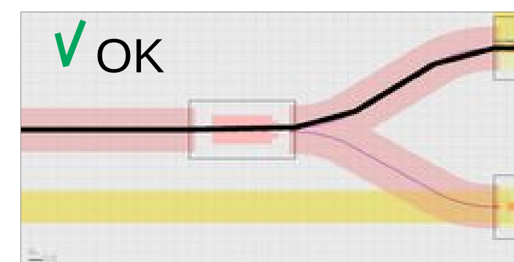


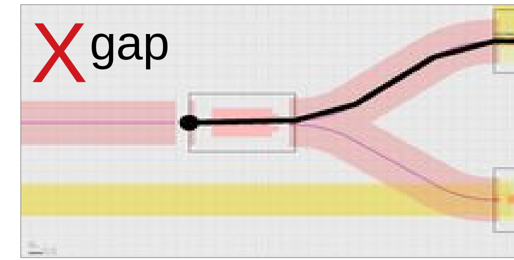






path





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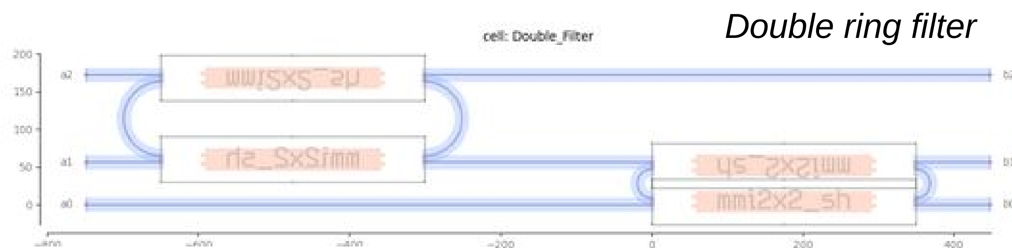
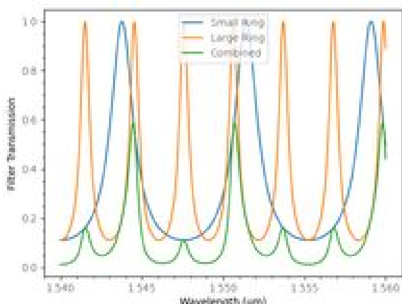
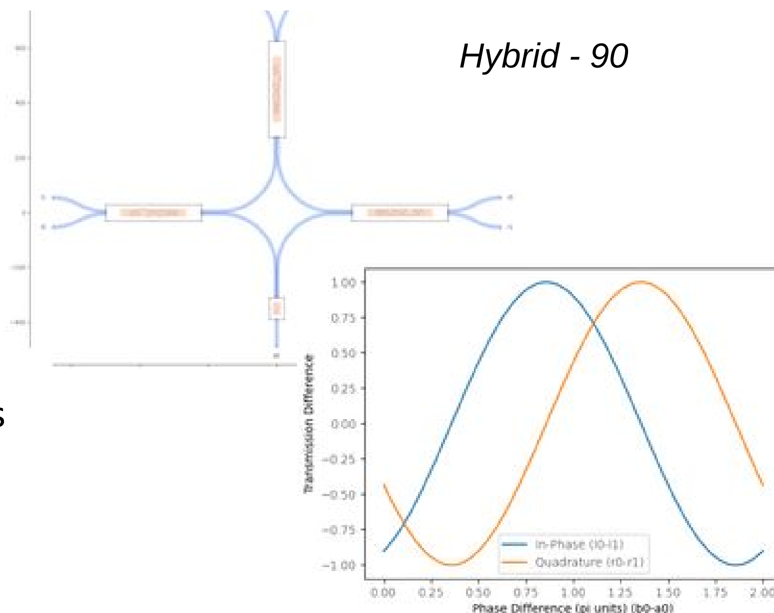
D. Design and validation in GDS: circuit simulation and verification at GDS level

Double ring filter





Hybrid - 90



Examples:

- Investigation of filtering characteristics
- Transmission simulation of a circuit
- Integration of Material models in PDK and components S-matrices

www.nazca-design.org

D. Design and validation with Nazca-Design

Tape-out of MASSTART inter- and intra- Data Center PICs using LETI and TEEM PDKs in Nazca

Thank you!

Contact: info@BrightPhotonics.eu

- ✔ Supply chain development
- ✔ PIC concepts & IP blocks
- ✔ Prototyping & Design
- ✔ PDKs

MASSTART team:
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Katarzyna Ławniczuk
Ronald Broeke