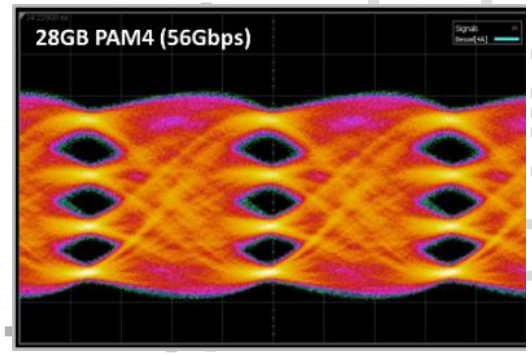
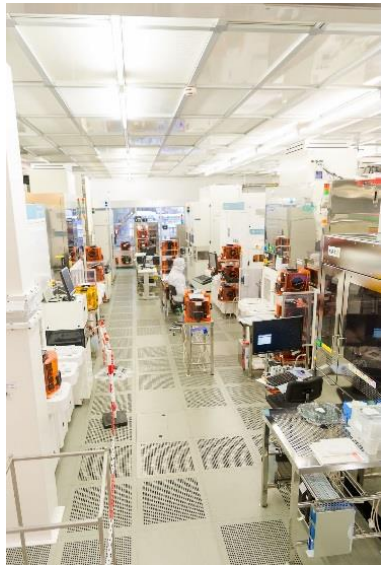


ADVANCED SILICON PHOTONICS PLATFORM FOR HIGH DATA RATE TRANSCEIVERS

Photonics Days Berlin Brandenburg | **Quentin Wilmart**, Stéphane Bernabé, Bertrand Szelag |
05.10.2021

LETI, TECHNOLOGY RESEARCH INSTITUTE



CEA-Leti founded in 1967, based in France (Grenoble)

1900
People

60
Startups created

>2760
Patents in portfolio

315 Million €
Budget

8,500 m² CLEAN ROOMS for 200mm & 300mm wafers

Optics and Photonics Division

Created in 1978
300 researchers, engineers and PhD students

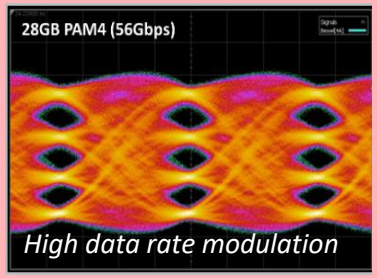
500 patents in portfolio
80 new patents per year

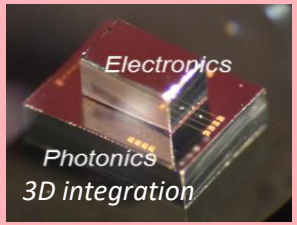
65 M€ budget
90% from external revenue

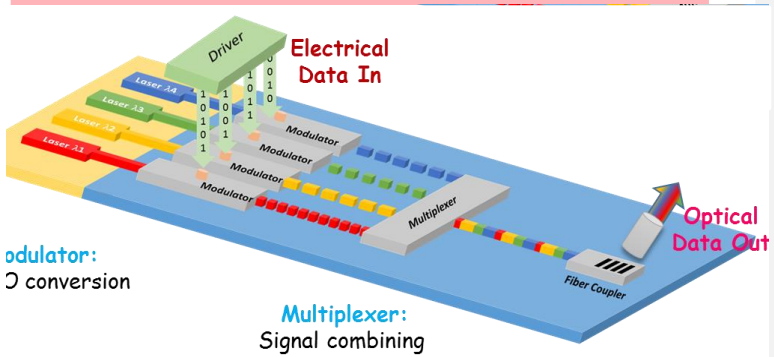
SILICON PHOTONICS TECHNOLOGY APPLICATIONS

High-speed interconnects for optical communications

- Telecom
- Datacom
- Computercom



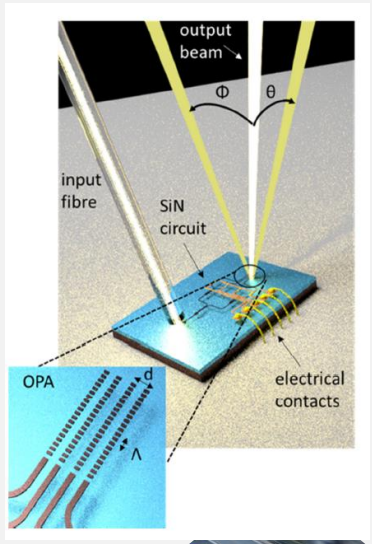




Szelag et al. SSDM 2018

Sensing

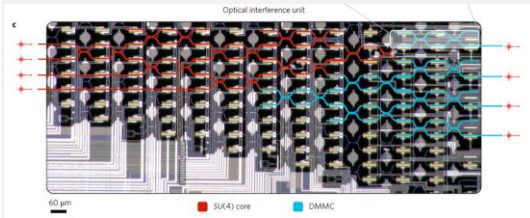
- Solid state beam steering OPA for LIDAR
- Tunable lasers for fiber optic sensing interrogator



N. A.Tyler et al. Optics Express 2019

Neuromorphic photonics

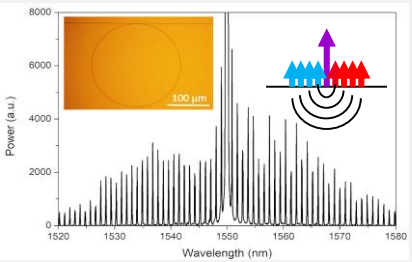
- Neuromorphic computing for AI



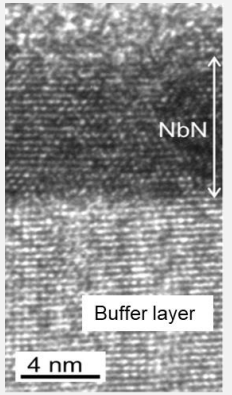
Linear operation (matrix multiplication) with large Mach Zehnder arrays

Quantum photonics

- Secured communications
- Quantum computing



Demonstration of photon entanglement
F.A. Sabattoli et al. ICTON 2019



NbN deposition on SOI

See session (Thursday 7th): *Photonic integration as quantum enabling technology*

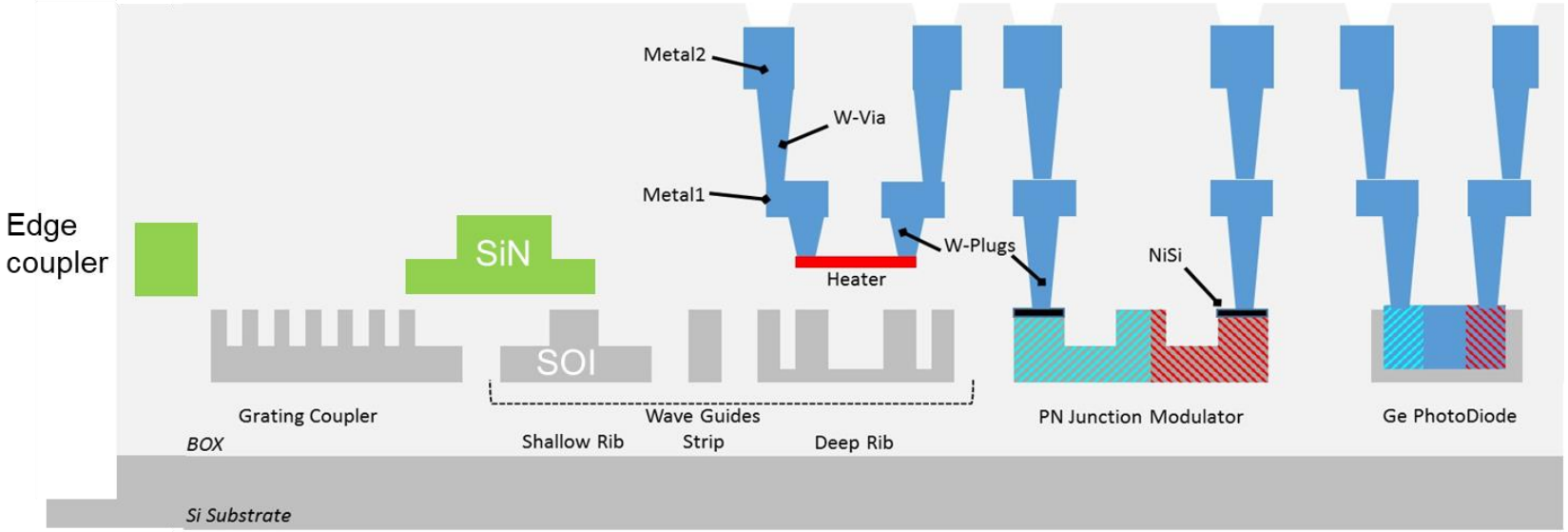
OUTLINE

1. Silicon photonics platform
   - Fabrication insights
   - Passive & active device library
2. Advanced building blocks
   - Ultra-low loss silicon waveguides
   - 3D photonics : Si-SiN platform
   - Wafer level test of edge coupling
   - Ultra low loss SiN platform
3. Conclusion

TECHNOLOGY KEY PROCESS FEATURES

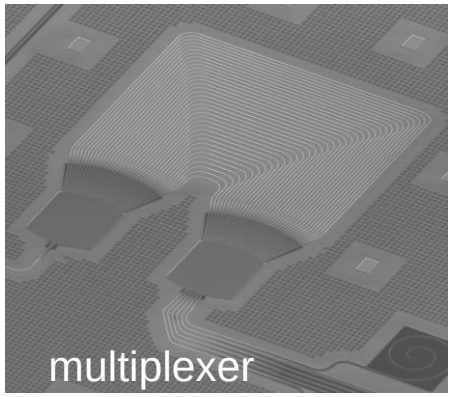
- **Advanced 300mm Si platform**
  - Substrates : SOI 310nm and 220nm
  - Si patterning with immersion lithography
  - 60nm smallest feature size
  - > 200 steps ; 24 litho levels
  - 40 metro/control steps
  - Low optical losses: 0.6-2 dB/cm
  - **Versatility**: combine building blocks

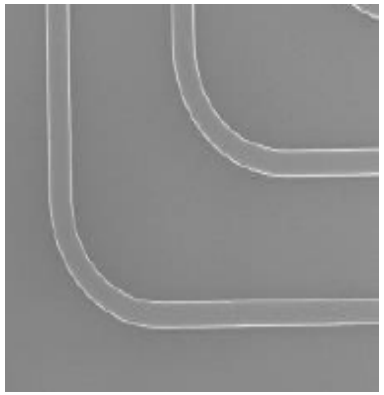
- **Process building blocks**
  - Multilevel silicon patterning
  - PN Silicon junctions
  - Germanium
  - PECVD SiN waveguides
  - Integrated resistance (heater)
  - Integrated laser (direct bonding of III-V wafers/dies)
  - Planarized BEOL : 2 AlCu routing levels

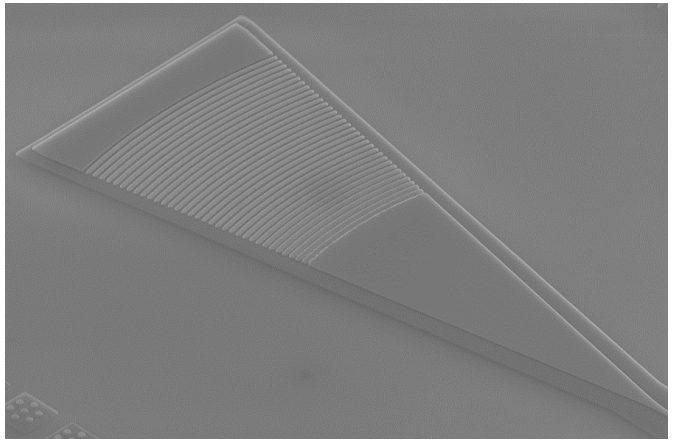


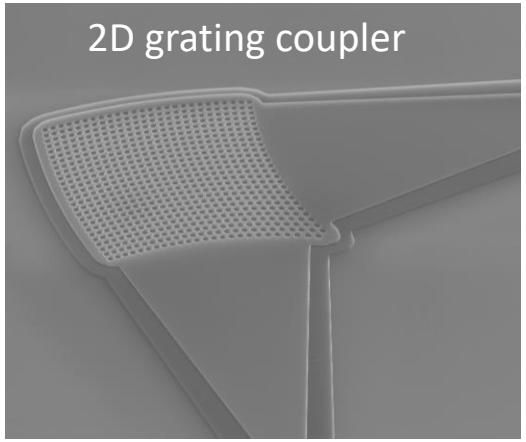
DEVICE LIBRARY: PASSIVE

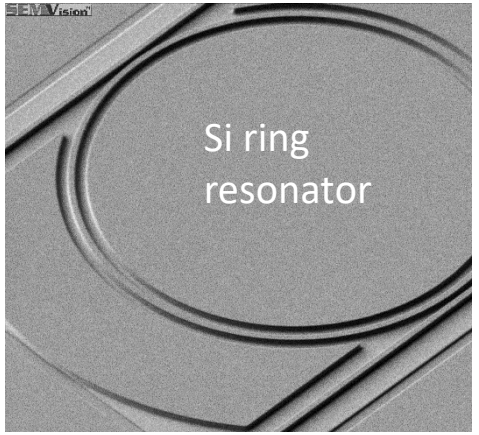
- Routing (waveguides, bends, crossings, splitters, MMI…)
- Wavelength Management
- Polarization Management
- Fiber Coupling
- DC phase shifter (with heater)

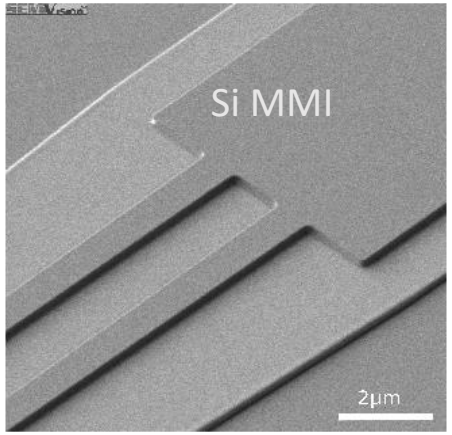










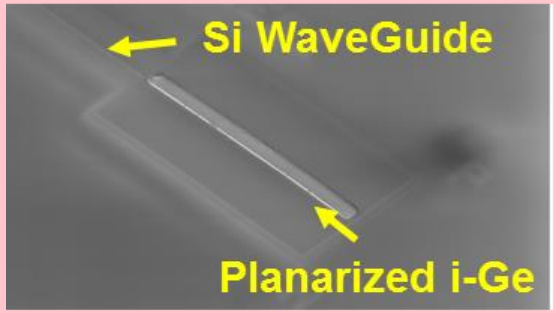


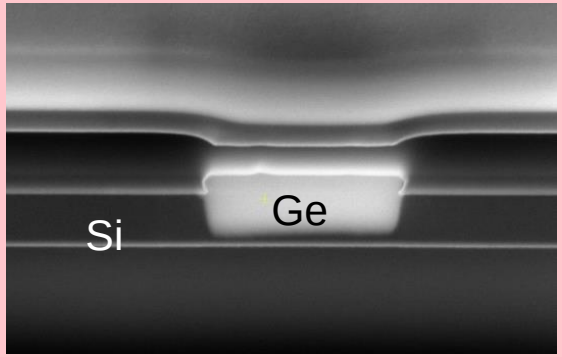
Components available through Process Design Kits (PDK), as layout (p-cells) & models

→ **MPW runs** @ *https://mycmp.fr/Si-310/*

DEVICE LIBRARY: ACTIVE

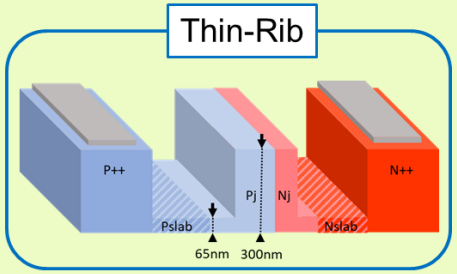
Ge photodiode

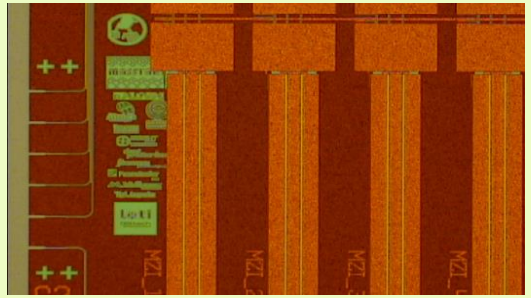


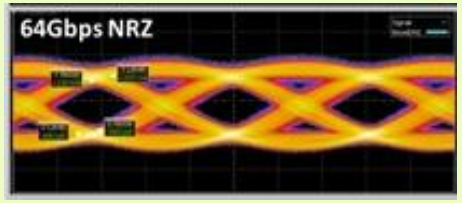


Responsivity	0.7 A/W
Dark current @ -2V	5 nA
BW @ -2V	> 35GHz

MZ modulators

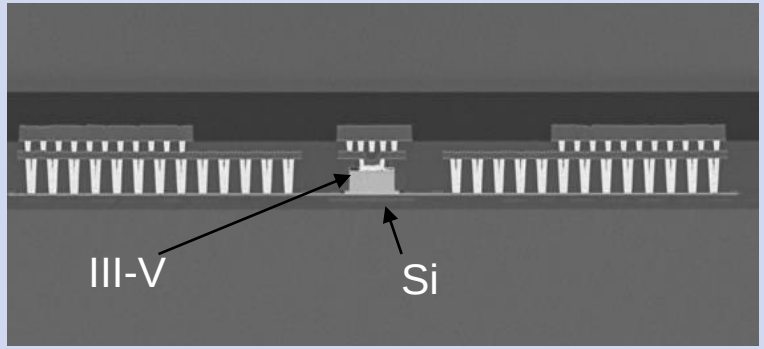


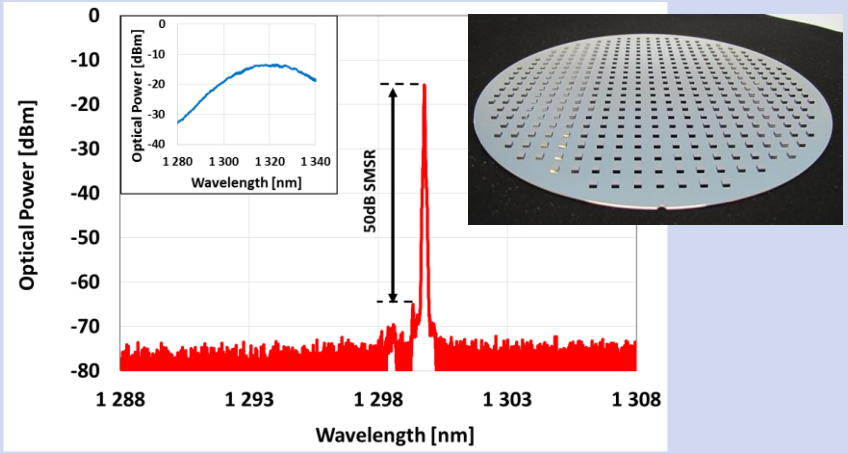




$V_\pi L_\pi$ @-2V (V.cm)	1.5
Losses (dB/cm)	7
BW@-6dB (GHz)	25

III-V/Si hybrid lasers





- ✓ 200mm CMOS compatible process
- ✓ Die bonding for multiple epitaxies

→ **MPW runs** @ *https://mycmp.fr/Si-310/*

(not in MPW)

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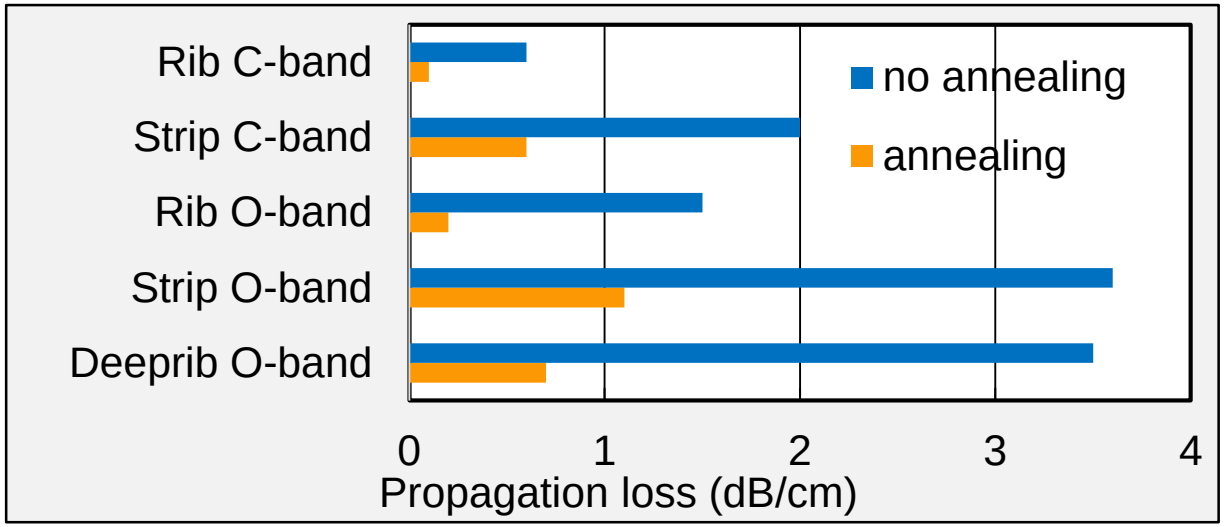
3 Conclusion

ULTRA-LOW PROPAGATION LOSS SILICON WAVEGUIDES (200MM)

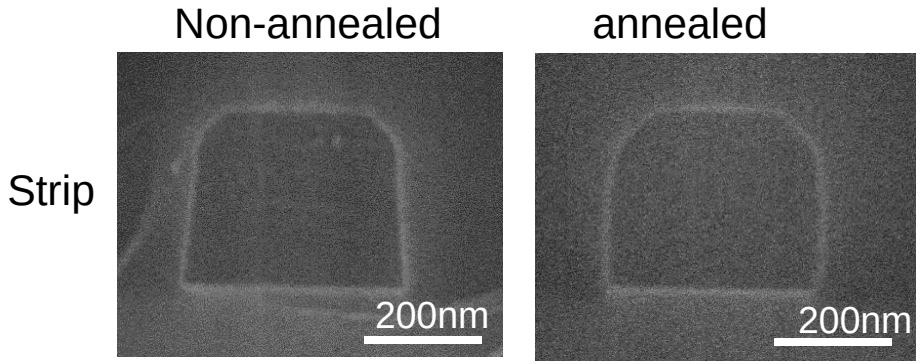
Low-loss Si waveguides:

- Roughness reduction with smoothing annealing (H2 850°C)
- Record low propagation losses in Si <1dB/cm
- ✓ No shape modification: no impact on other devices
- ✓ No impact on modulator efficiency

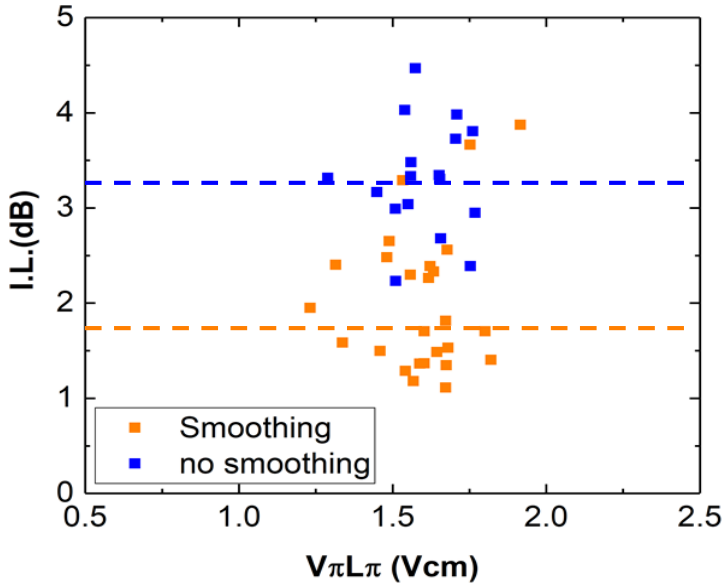
Strip WG @1310nm	1.1dB/cm
Strip WG @1550nm	0.7dB/cm

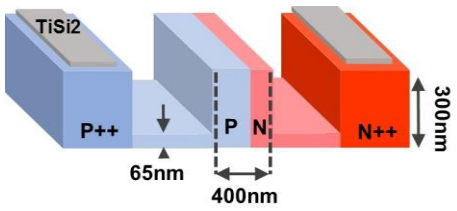


Q. Wilmart et al., Journal of Lightwave Technology (2021)

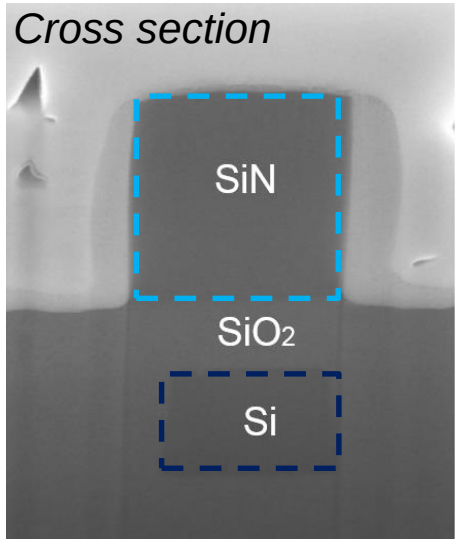


PN junction efficiency preserved
dBs of insertion loss improvement





ADD-ON: PECVD SILICON-NITRIDE



Why PECVD Silicon nitride:

- Low temperature deposition
- Low refractive index (n_{SiN} ~ 1.9)

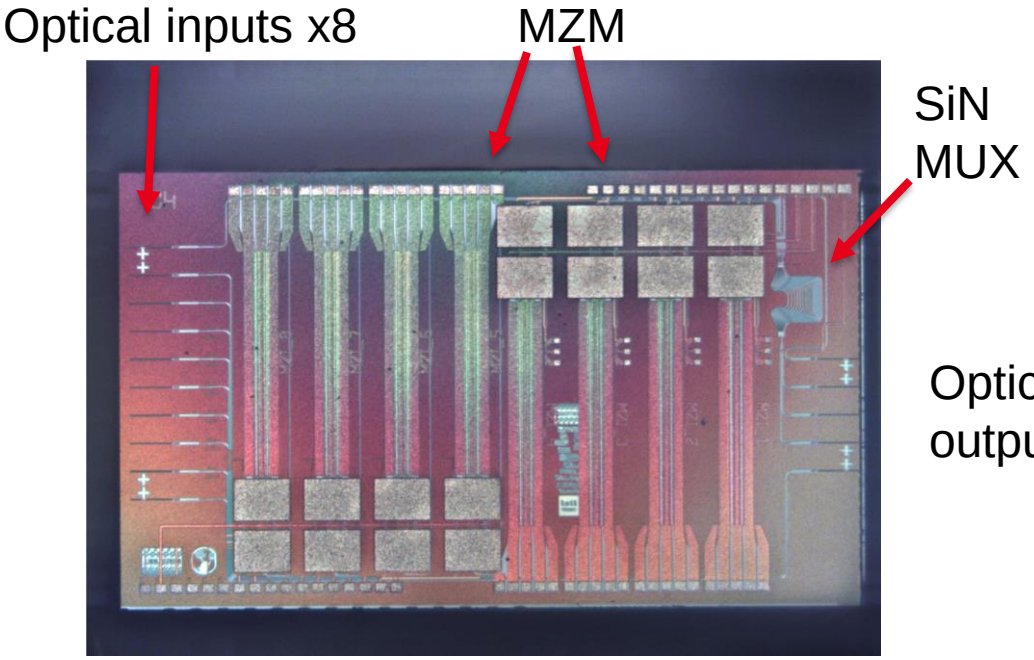
→ less sensitive to fabrication imperfections

Waveguide: 0.6dB/cm

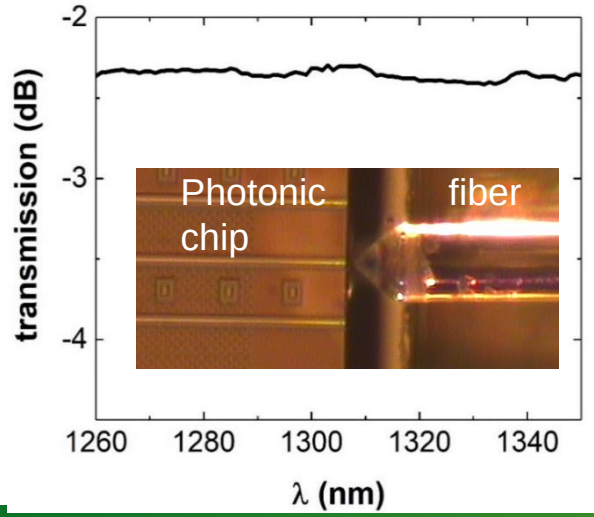
- Low thermo-optic coefficient (~$2x10^{-5}$ K^{-1})

→ Temperature quasi-insensitive **multiplexer**

- Broadband coupling scheme



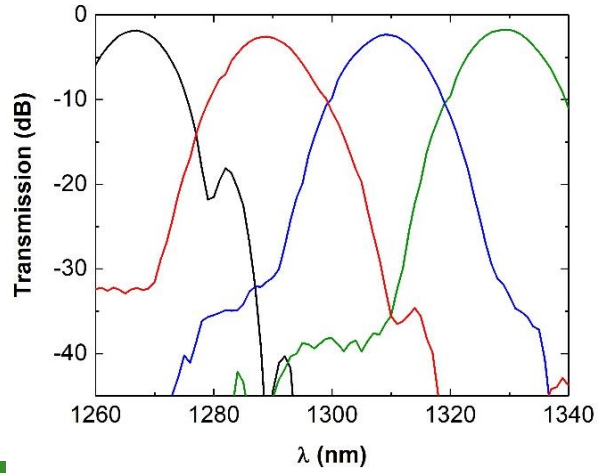
- SiN edge coupler



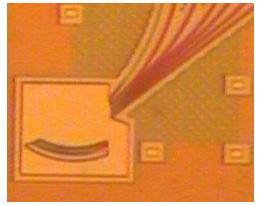
- CWDM multiplexer: SiN Echelles grating

I.L. < 2.5dB

Thermal shift: 13pm/°C



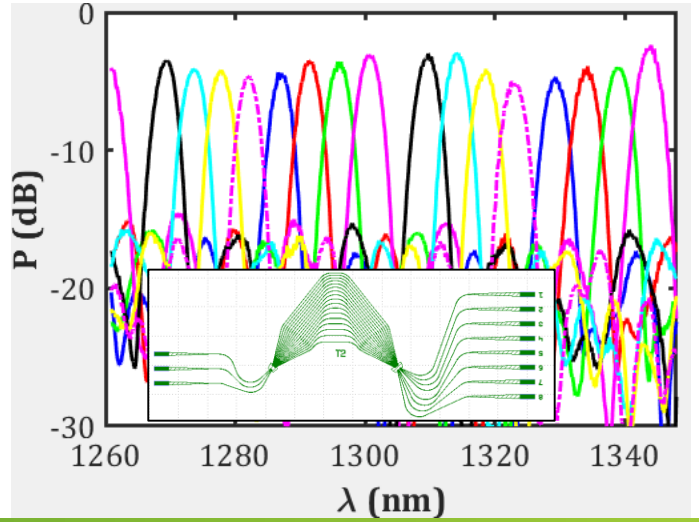
Q. Wilmart et al. , Applied Sciences 2019



- SiN AWG

8 channels – spacing: 800GHz

(design Bright Photonics)



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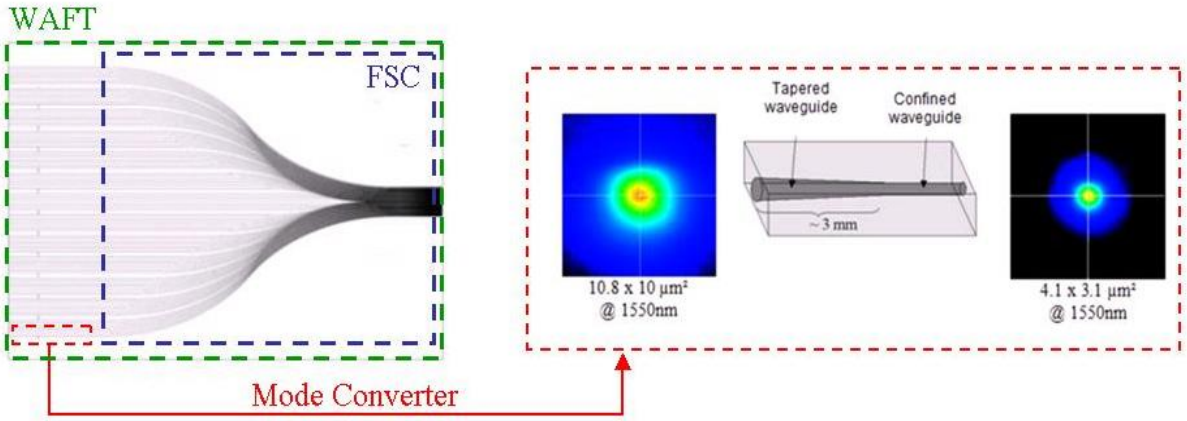
Wafer-level test of edge coupler

- Waveguide Array to Fiber Transposer (WAFT) fabricated by **Teems Photonics**

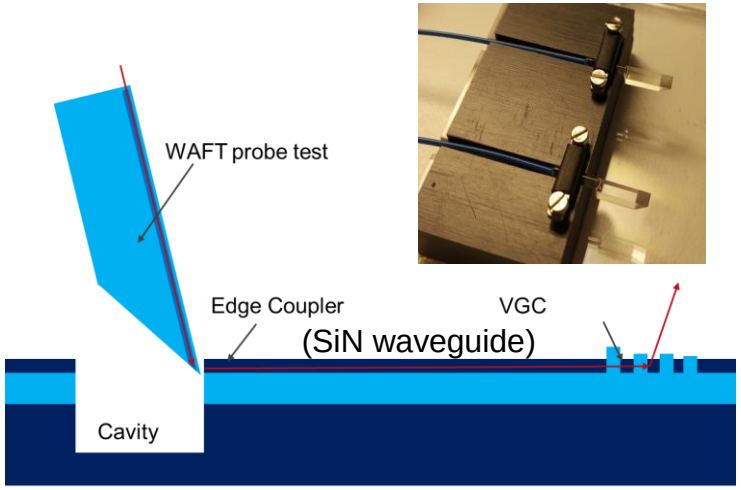
➢ DRIE cavity etching in PIC

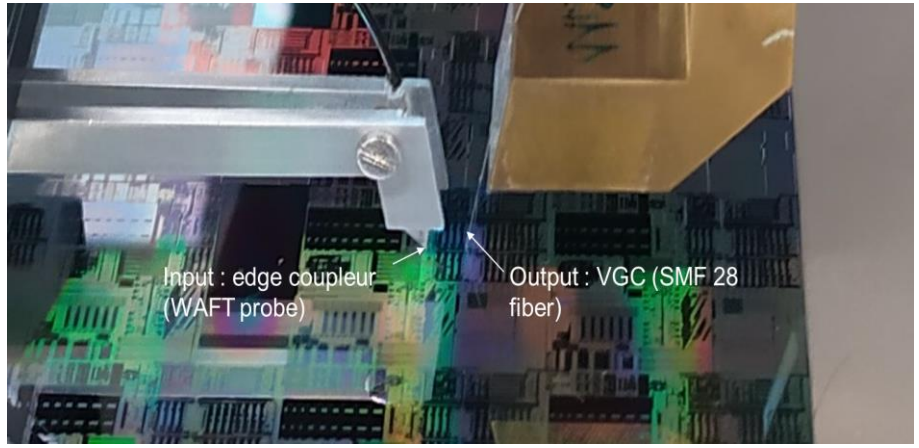
➢ Mode adaptor with WAFT: SiN tapered waveguide ↔ SMF28

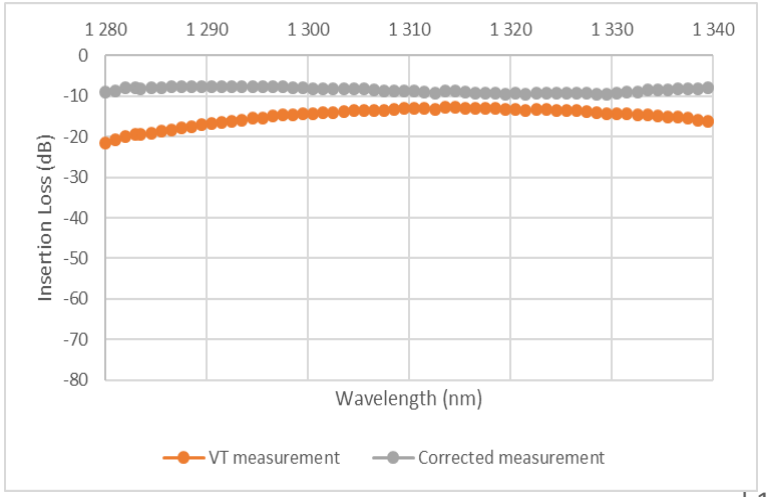
Down to 0.8dB loss for the WAFT – PIC coupling (diced chip test)



➢ Wafer Level Test of PICs with Edge Couplers







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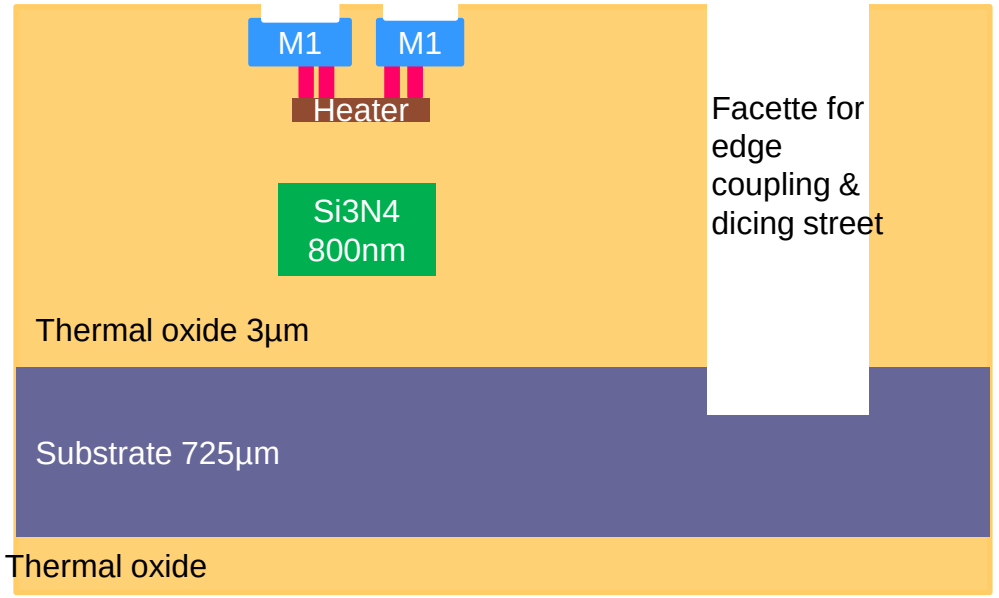
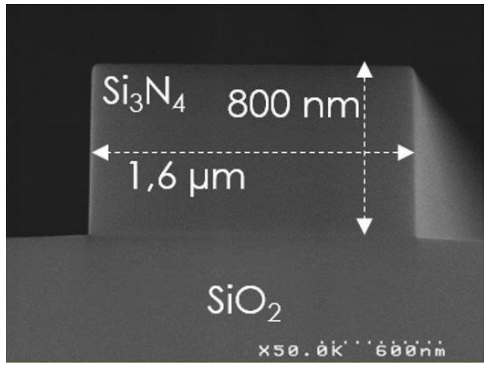
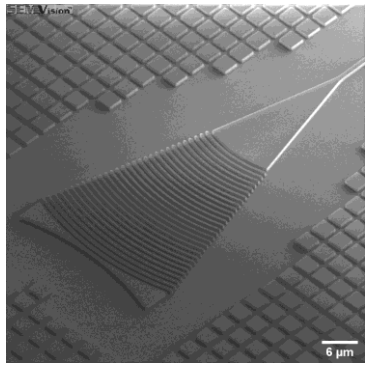
LPCVD SIN PLATFORM

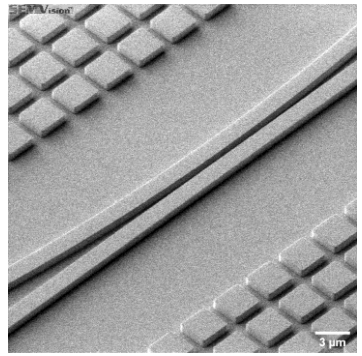
High quality LPCVD Si_3N_4

- Stoichiometric SiN
- 200mm wafers with subtractive process
- 800nm thick, (other thicknesses possible)
- Annealing for N-H removal and waveguide smoothing
- ➢ Ultra-low propagation losses @1550nm: 4dB/m
- ➢ Microring resonator with Q factor ~ 10^7
- High confinement ↔ compactness (20µm bend radius)
- Nonlinear optics: frequency comb generation
- PDK & device library
- ➢ **MPW runs:** *https://mycmp.fr/Si3N4-800/*









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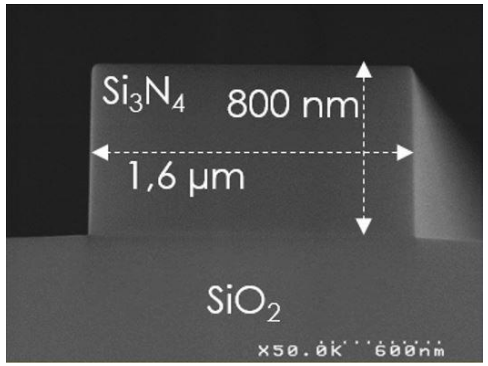
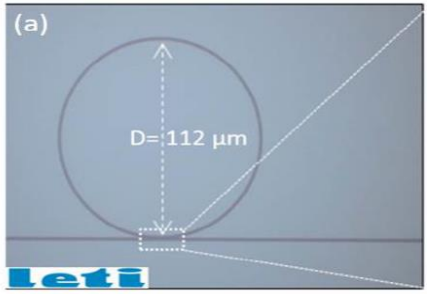
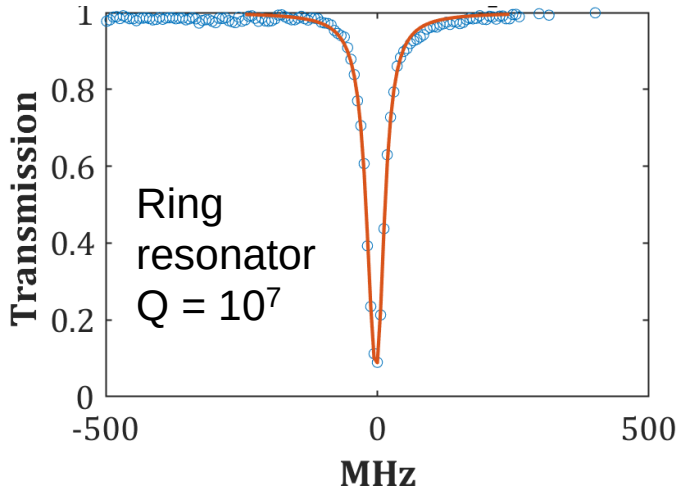
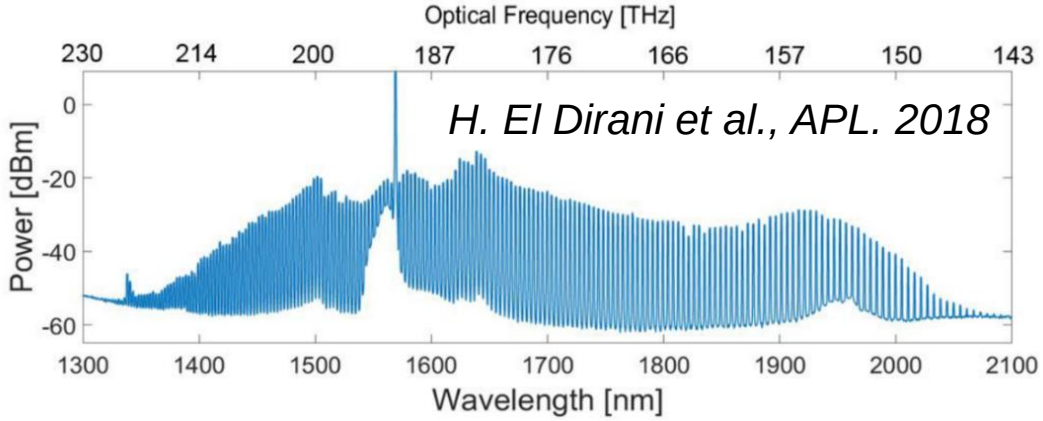








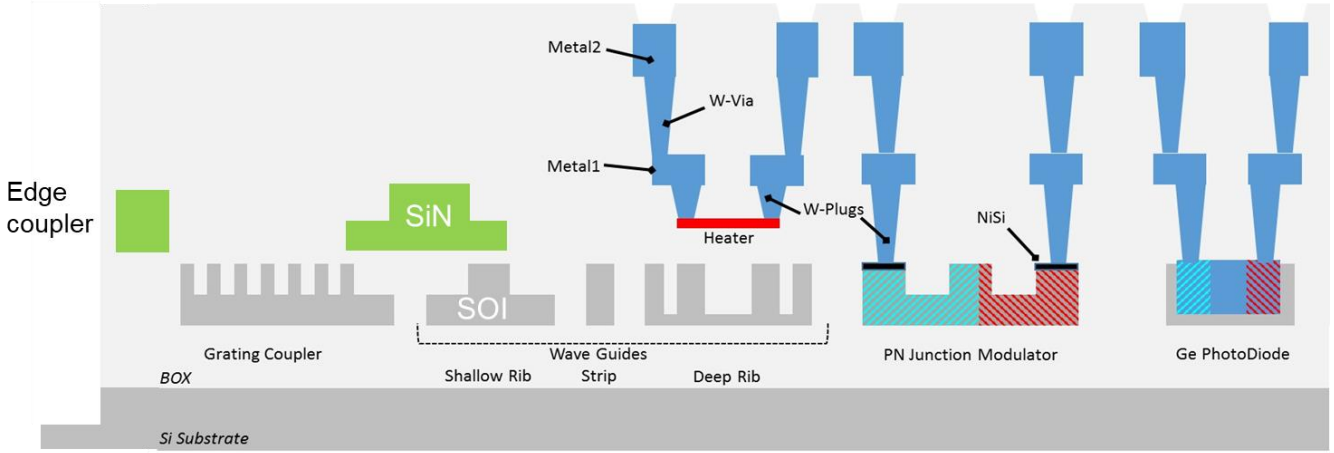
Nature 2017 : 50 Tbps demo

Microresonator-based solitons for massively parallel coherent optical communications

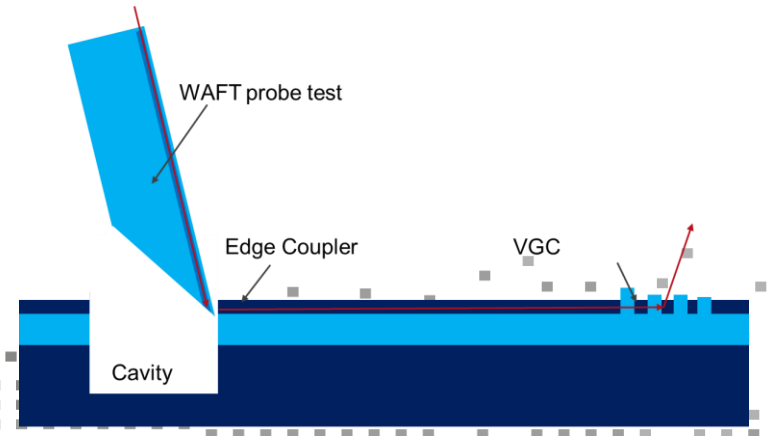
Pablo Marin-Palomo[1]*, Juned N. Kemal[1]*, Maxim Karpov[2]*, Arne Kordts[2], Joerg Pfeifle[1], Martin H. P. Pfeiffer[2], Philipp Trocha[1], Stefan Wolf[1], Victor Brasch[2], Miles H. Anderson[2], Ralf Rosenberger[1], Kovendhan Vijayan[1], Wolfgang Freude[1,3], Tobias J. Kippenberg[2] & Christian Koos[1,3]

Future of datacom?

CONCLUSION



- 300mm Si photonics platform
- PDK with device library → MPW runs
- Highlights: Si/SiN integration & wafer level test of edge couplers
- Si_3N_4 LPCVD platform with ultra-low propagation losses → frequency comb generation



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