

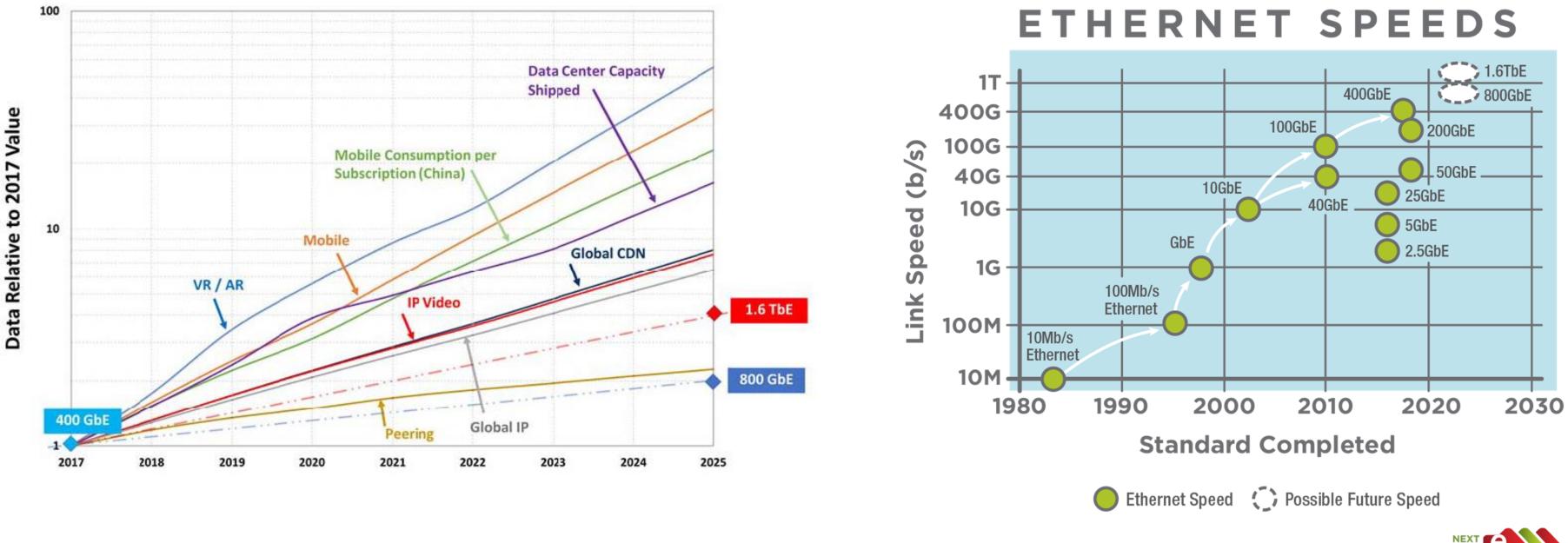
TERABIT TRANSCEIVERS FOR THE DATACENTER AND HIGH - VOLUME MANUFACTURABILITY

Boaz Atias, 5 October 2021 Photonics Days Berlin Brandenburg 2021





BANDWIDTH DEMAND IS GROWING - NEED FOR SPEED



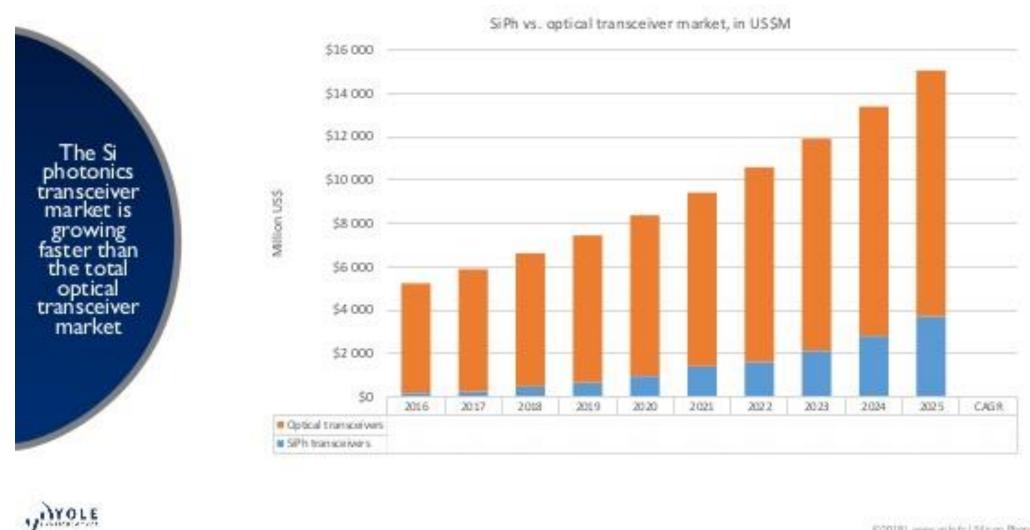
- DC bandwidth demand grows exponentially
- 400G interconnects now ramping up
- 800G and 1.6T standards & MSAs in the pipeline





MASS MARKET? MASS MANUFACTURING

SI PHOTONICS VS. LEGACY OPTICAL TRANSCEIVER FORECAST, IN VALUE



- **Transceivers are turning into a multi-Bn market**
- **Reaching critical mass to leverage cost savings of silicon photonics (10s M units)**

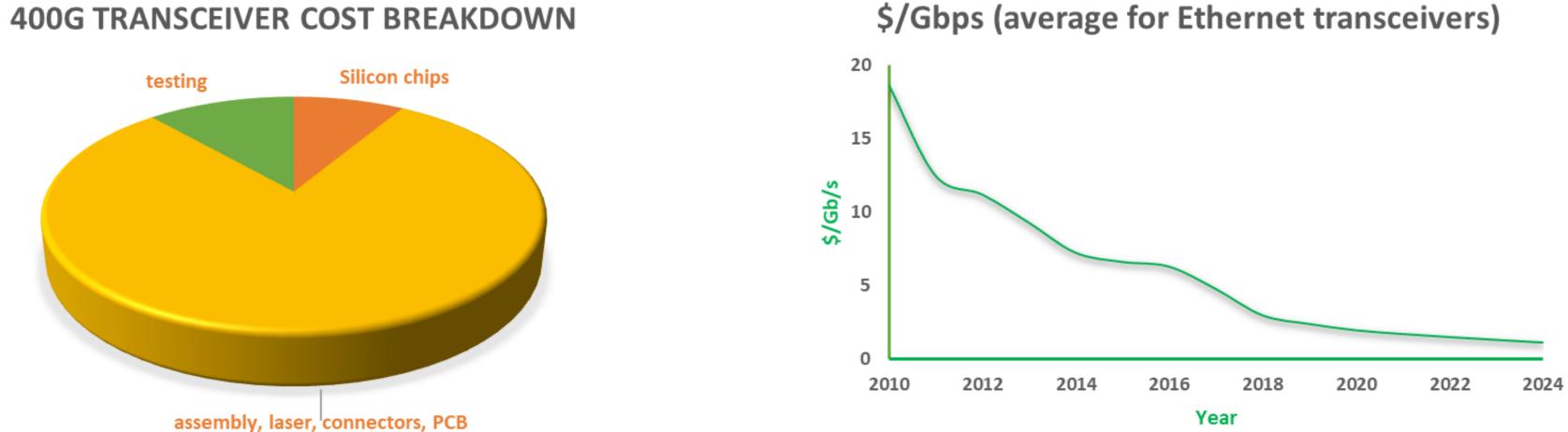
(C2018) www.sule.tr.| Silican Phasanes 2018 | Sample



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THE PACKAGING CHALLENGE



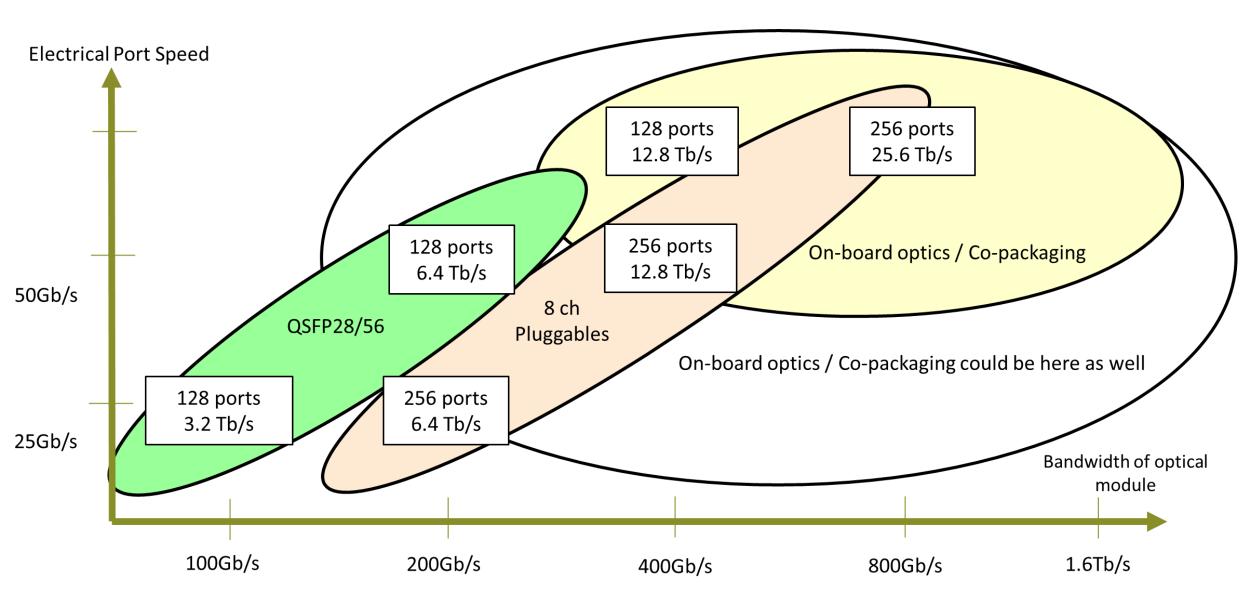
- Transceiver costs are dwarfed by assembly & packaging costs
- **Cost/bit drops to enable deployment of new generation transceivers**
- **Existing scaling model relies on low-wage production**
- **Current approach reaching its limits**





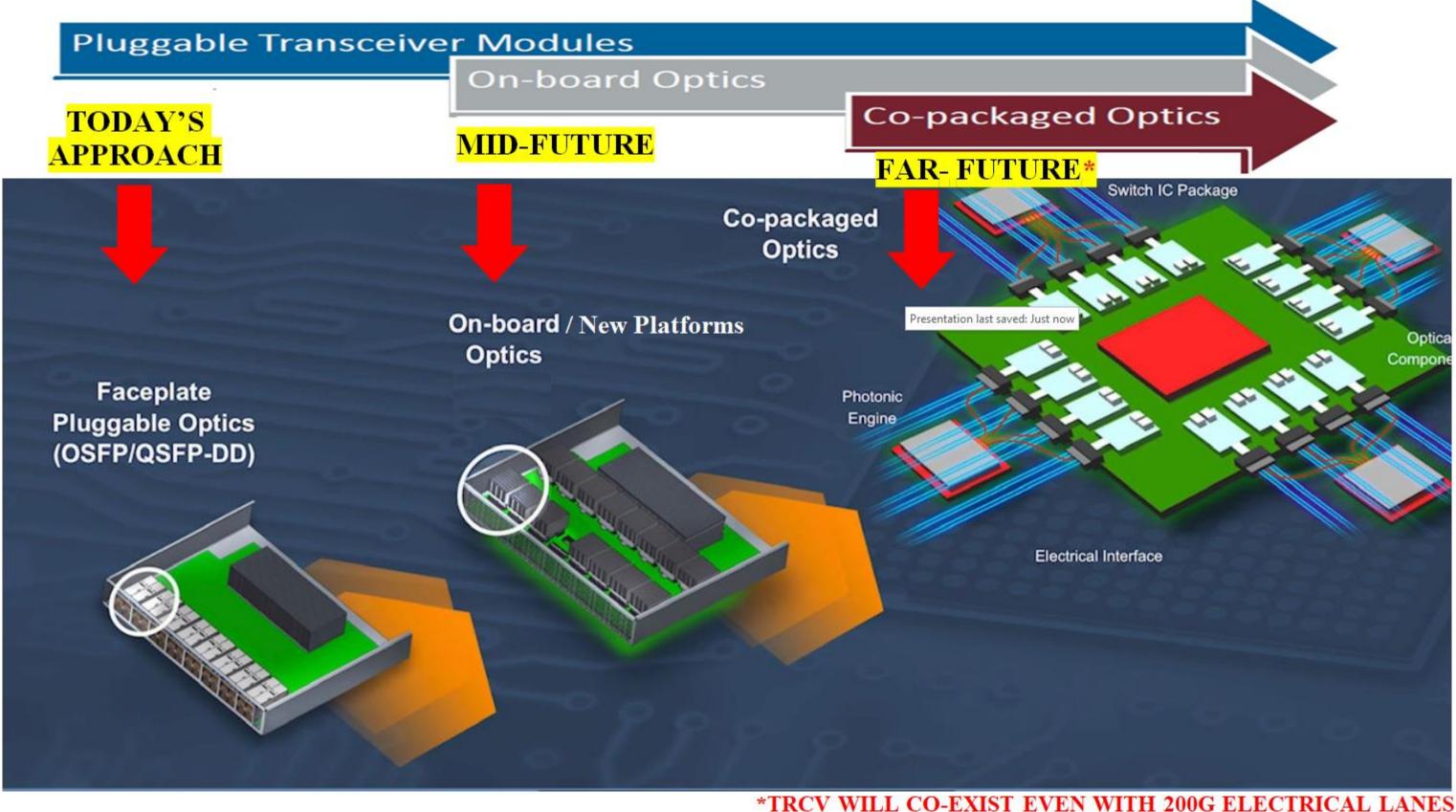


THE ROAD TO TERABIT/S TRANSCEIVERS#1



- 100G/lane optics now ramping up
- 100G electrical ports introduced (100G SERDES)
- Speed evolution paradigm:
 - increase #lanes with existing optics
 - move to higher speed/less lanes
- 800G modules (25.6T switches) will use pluggables
- Terabit modules will migrate to new form factors
- Next coming rate is 200G/Lane... MASSTART#2...?

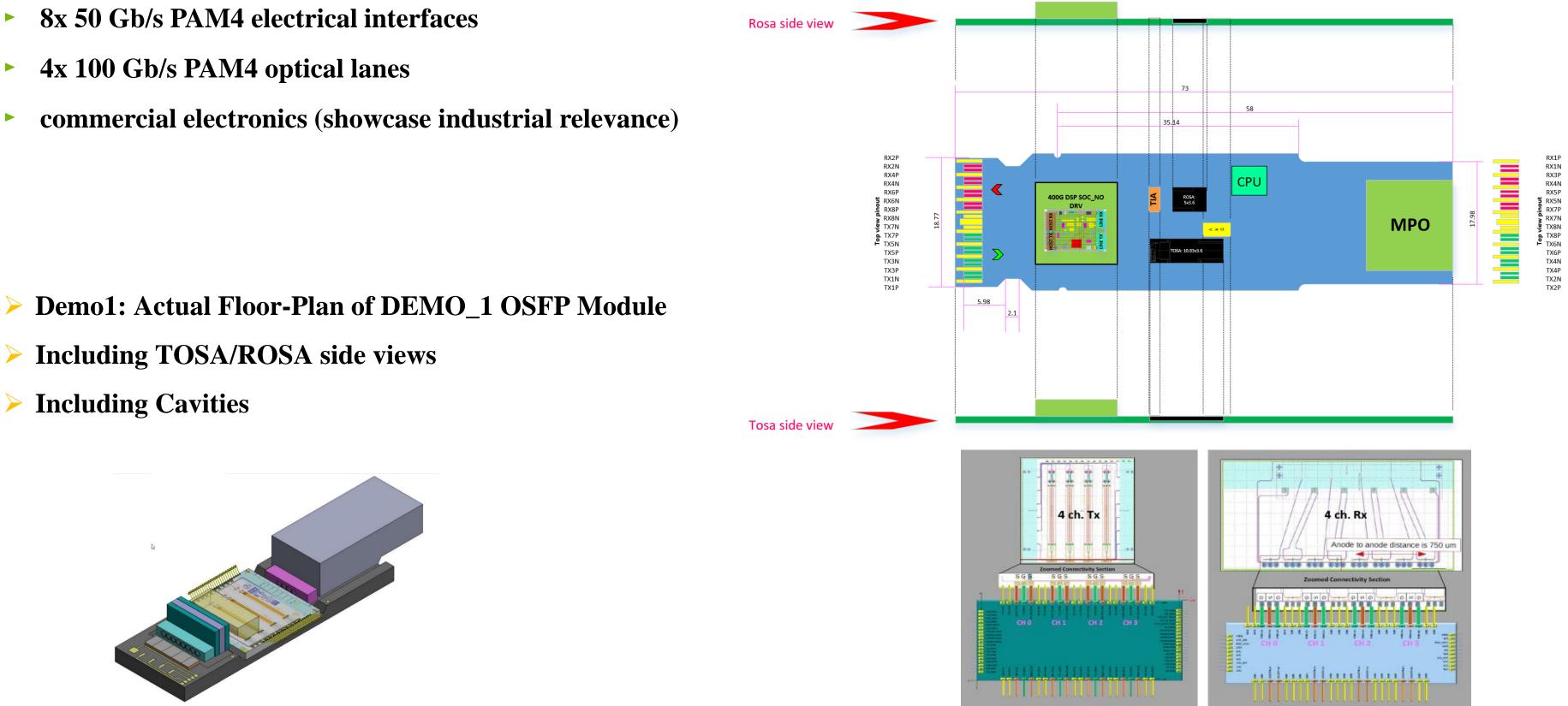
THE ROAD TO TERABIT/S TRANSCEIVERS#2





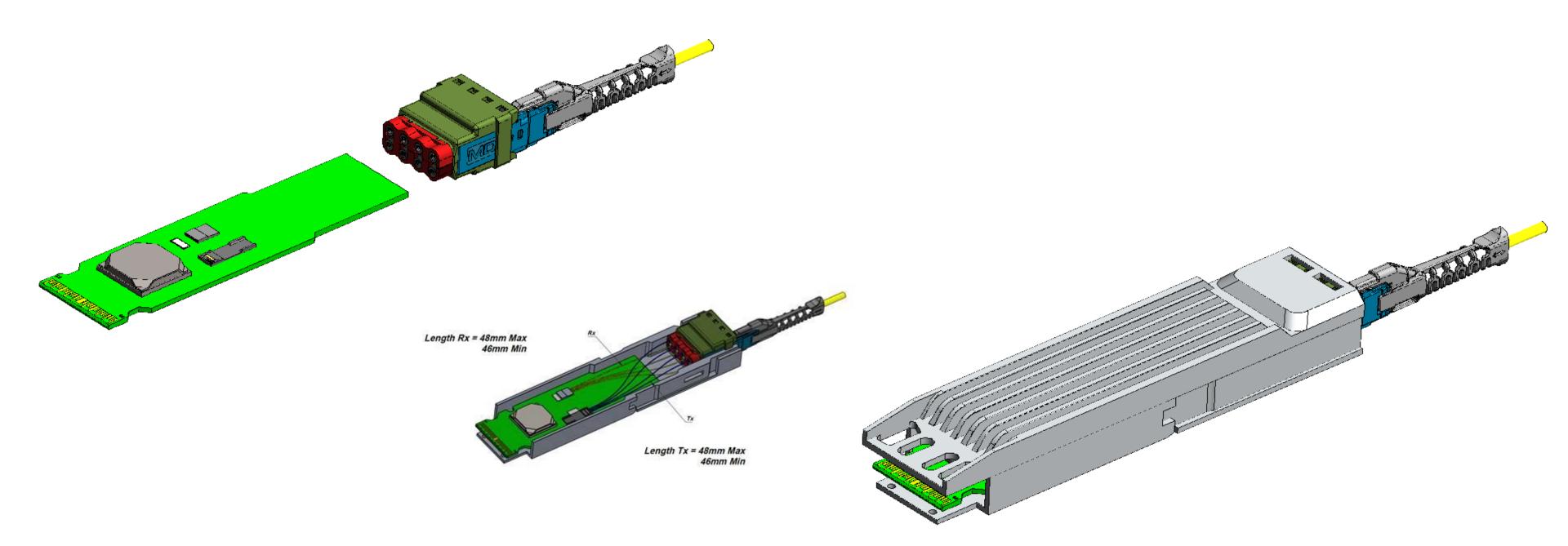
MASSTART PROTOTYPE 1

Pre-alpha 400GBASE-DR4 transceiver



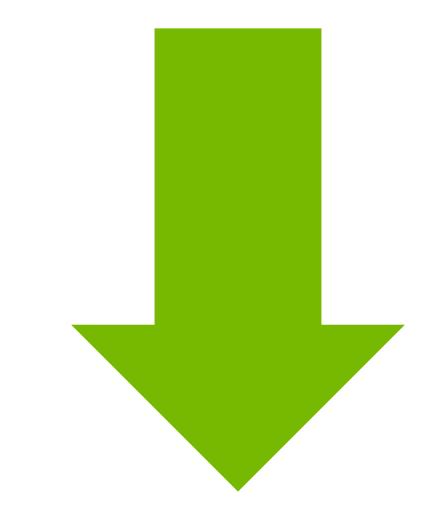
🥺 NVIDIA

FORM FACTOR [3D MECHANICAL DESIGN OSFP]





The Road To MASSTART and Mass-Production



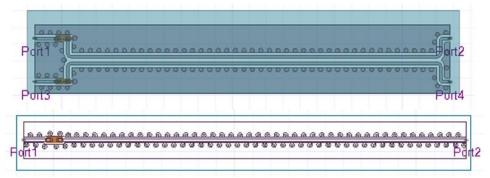


High speed simulations\Topologies and Materials#1

Material candidates

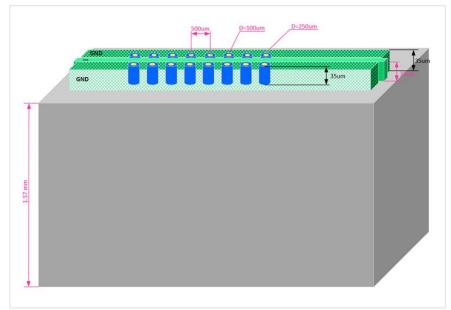
Material	DK	DF	3 dB length @50GHz	3 dB length @60GHz
Roger 3003	3	0.001	<38.1mm	<30.48mm
Roger 1200	3.05	0.017	~38.1mm	~30.48mm
Megtron 6	3.7	0.0067	~25.4mm	~20.32mm
FR4	3.9	0.018	~15.24mm	~12.7mm

Simulation Topology

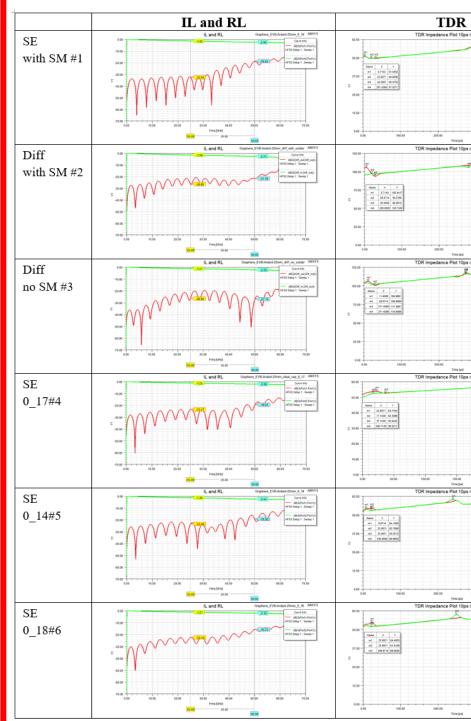


- Frequency Domain: IL/RL/TDR
- Time Domain:
 25GNRZ/50GNRZ/26GBAUD/53GBAUD
- Topologies-2 Approaches:
 SE [W/WO Solder mask] 4 different Topologies
 Diff [W/WO Solder Mask]
- 2 different Materials MEGTRON6 and Rogers3003

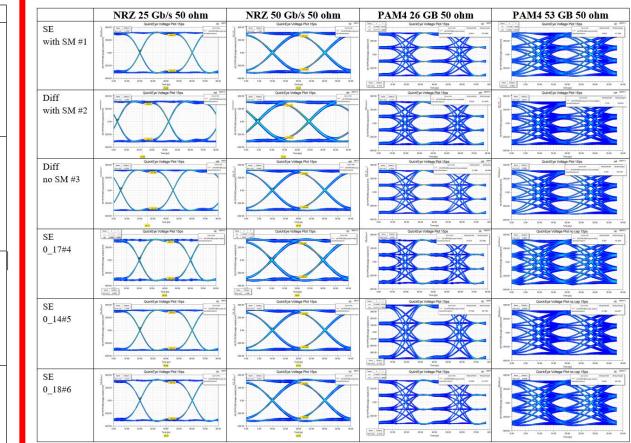
PCB Topology – Cross-section view

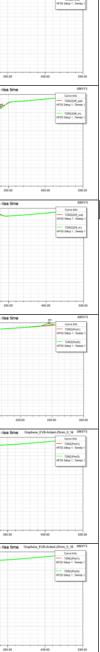


Frequency Domain simulations result



Time Domain simulations result





10

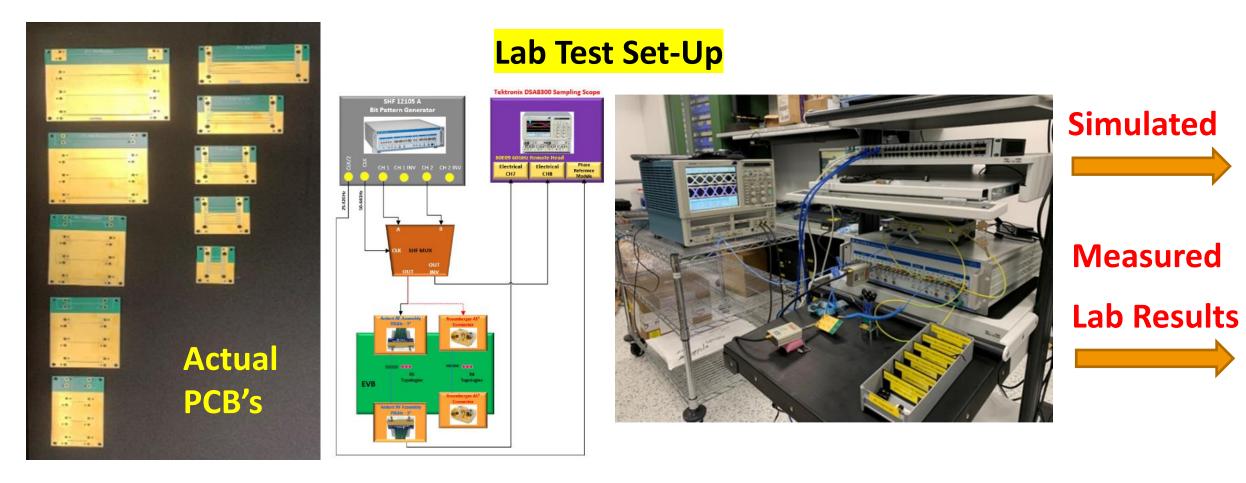
Test Boards to determine MASSTART Prototypes TLM SI – Towards Mass-Production

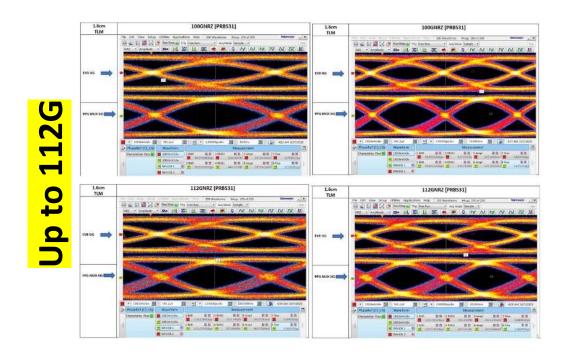
Overall, simulated, designed ,manufactured and tested:

6 different Topologies X 2 different Materials X 6 different TLM lengths X 2 Different Connectors

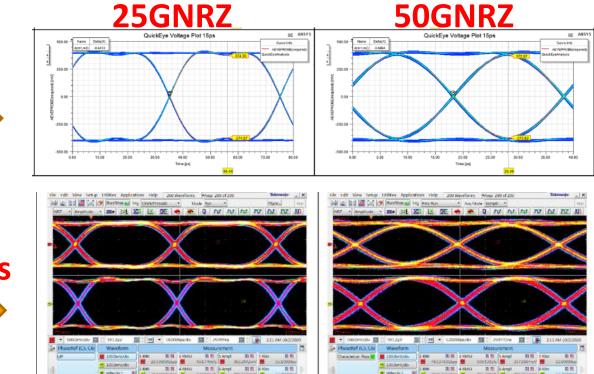
so, the overall Matrix of the TLM should give a good insight for the future,

while defining the final Layout design of MASSTART Prototypes





Simulation vs. Reality- [Time Domain]

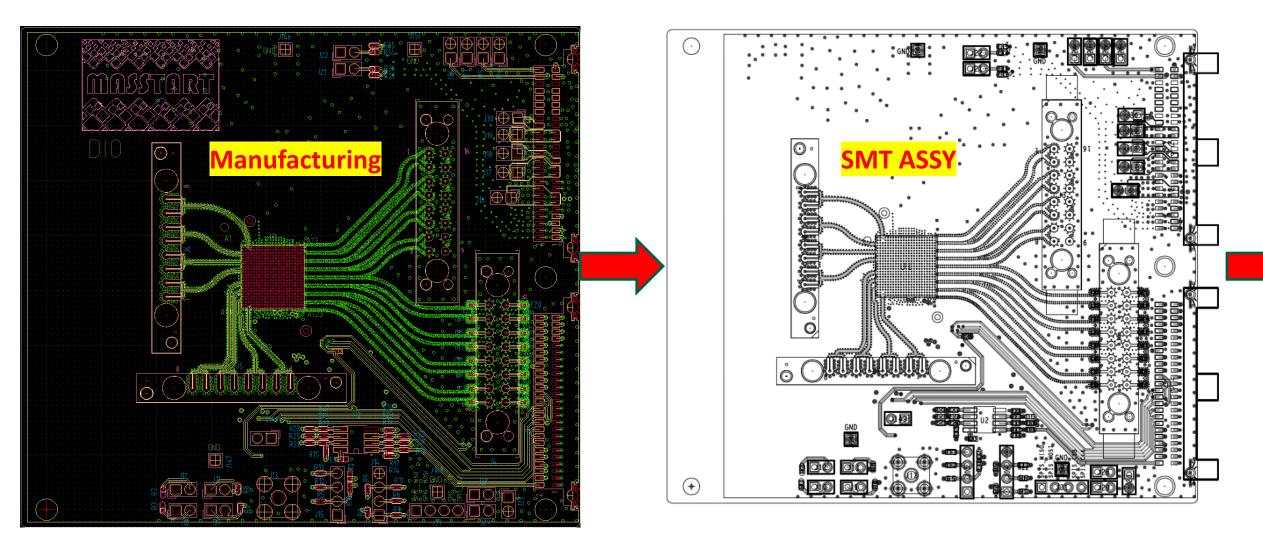


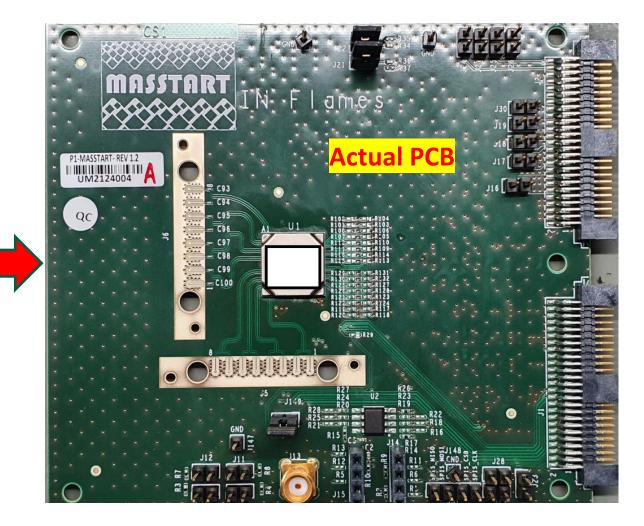


PRE-ALPHA 400GBASE-DR4 TRANSCEIVER – PCB DEMONSTRATORS

Pre-alpha 400GBASE-DR4 transceiver - progress

- **Floorplans designed for QSFP-DD and OSFP form factor**
- Layout for an open platform EVB designed
- **DSP** platform tested and modelled
- SiPh chips in fab, assembly starting Q3 2021

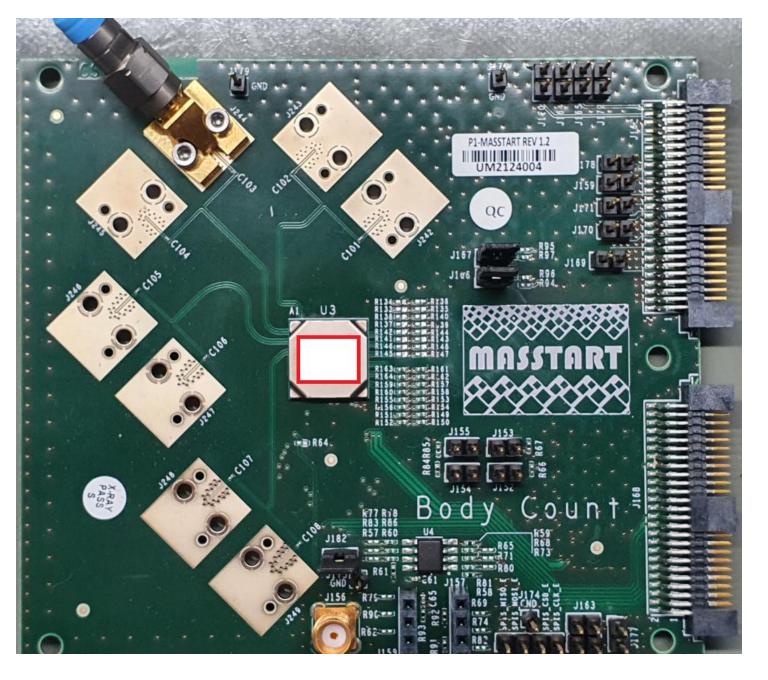






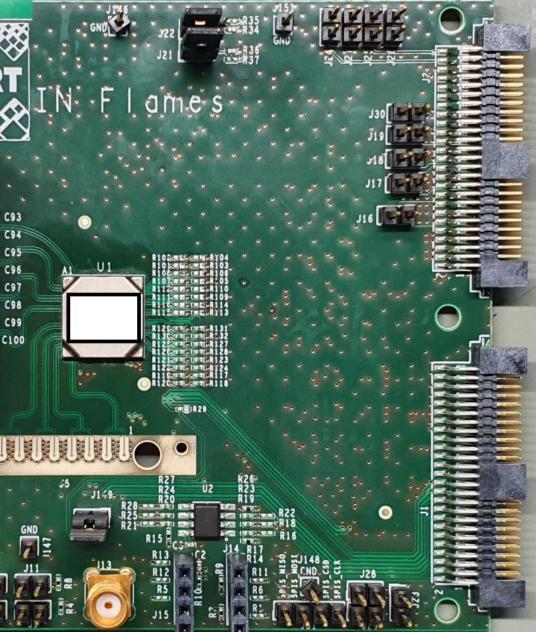
PRE-ALPHA 400GBASE-DR4 TRANSCEIVER – PCB DEMONSTRATORS

Rosenberger Based Prototype



P1-MASSTART- REV - C95 - C96 - C97 - C98 m C99 - C100 0

Ardent Based Prototype

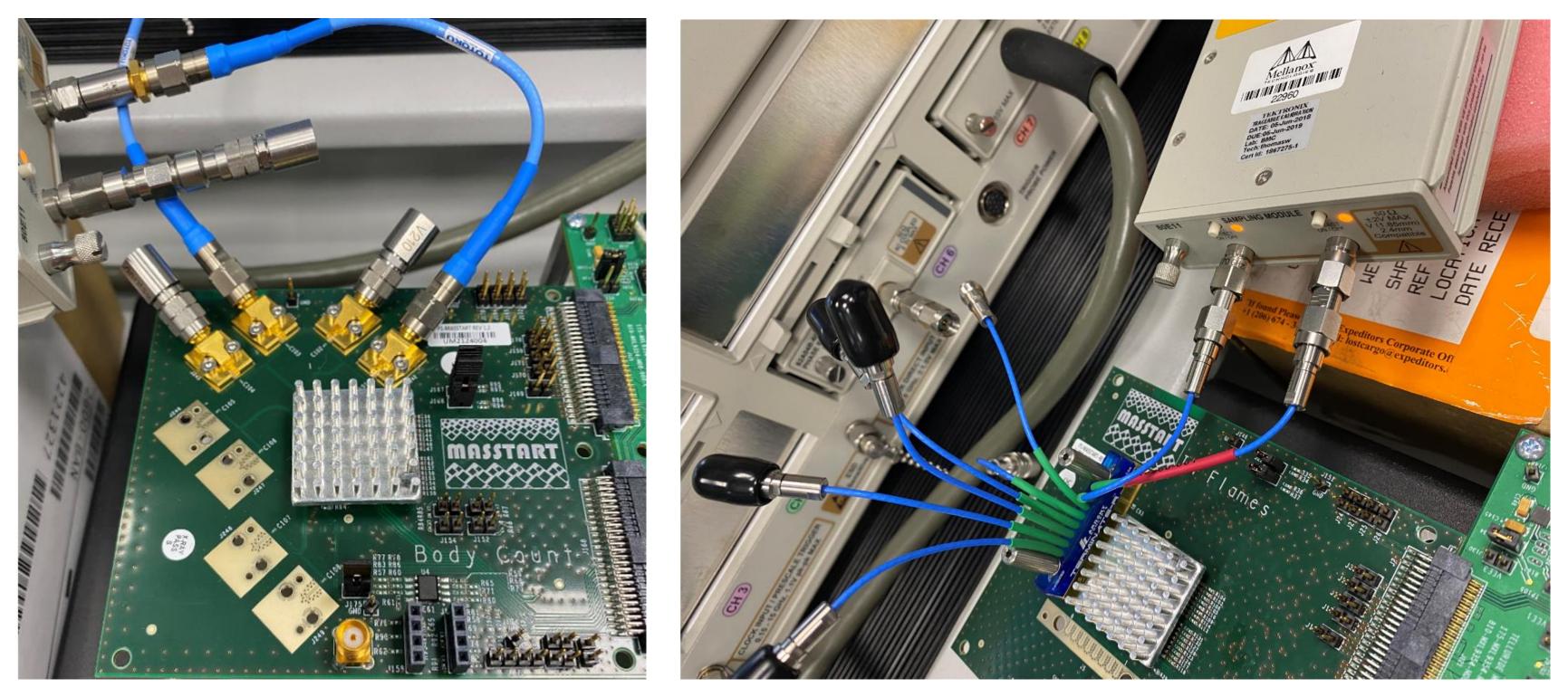




PRE-ALPHA 400GBASE-DR4 TRANSCEIVER – PCB DEMONSTRATORS

Rosenberger Based Prototype

Ardent Based Prototype



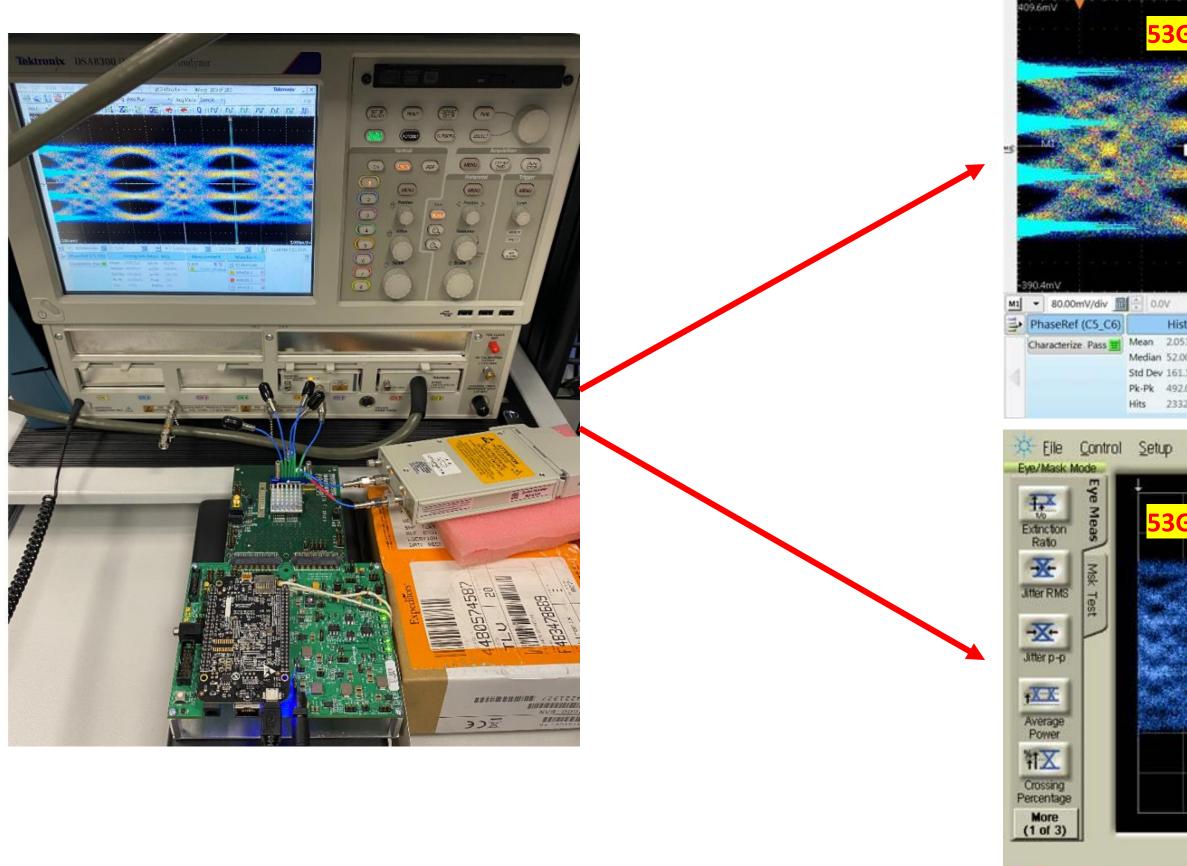


PRE-ALPHA 400GBASE-DR4 TRANSCEIVER – LAB RESULTS

NRZ · Amplitude · XXA

1) 2 Precision Timebase... Reference: 13.28125 GHz

Electrical Domain



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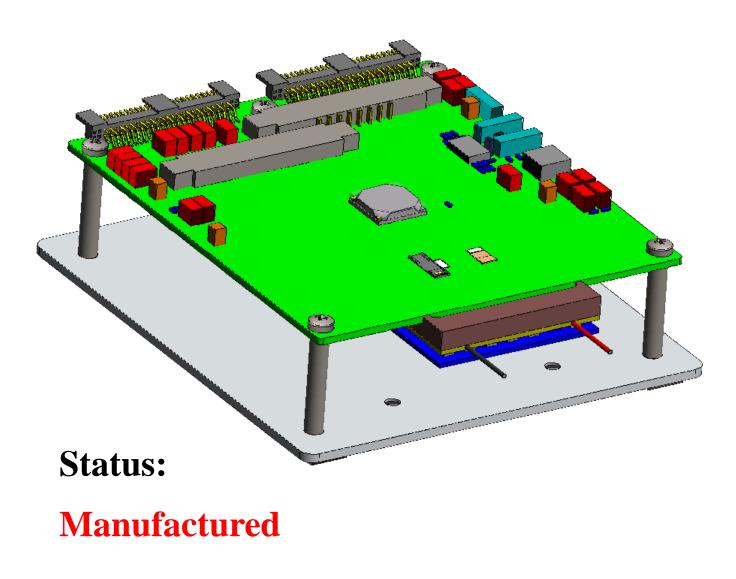
MASSTART OPTICAL/ELECTRICAL DEMONSTRATORS – MECHANICAL DESIGN

Two different 3D Mechanical design were designed manufactured using Micro Mechanical chip processing.

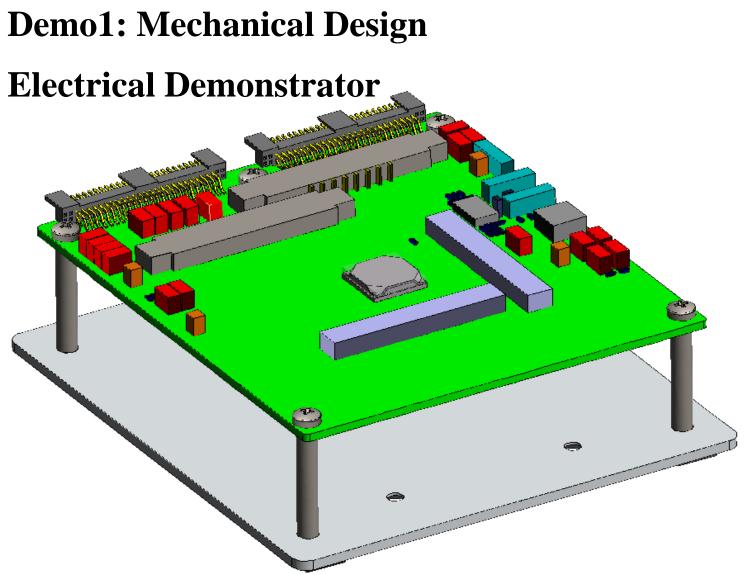
Since the Cavity for the TOSA/ROSA is based on mechanical cavity, on one flavor of the optical demonstrator (along with PCB) cutout) it was extremely important to ensure flexibility of adjustment on the Z-Axis, especially.

Flexibility on the X,Y Axis was ensured at the PCB cut-out design.

Demo1: Mechanical Design Optical Demonstrators



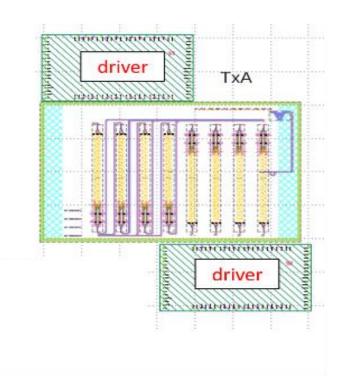
Electrical Demonstrator Status: Manufactured

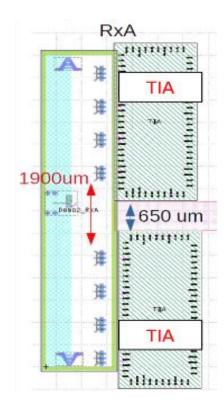


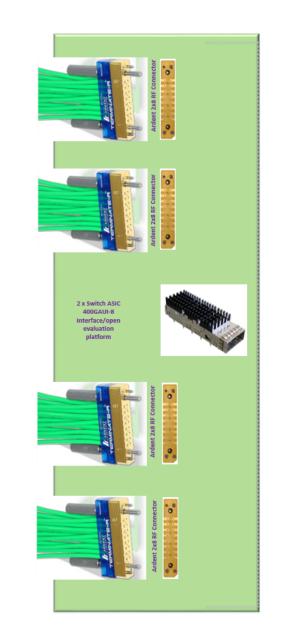


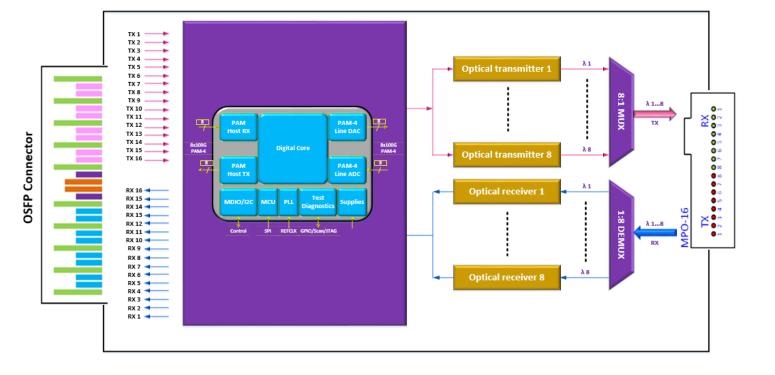
MASSTART PROTOTYPE 2 800G 8 Lane transceiver

- 8x 100 Gb/s PAM4 optical lanes
- LAN WDM optics (800 GHz)
- **Commercial electronics**
- **EVB** platform targeting pluggable/on-board optics









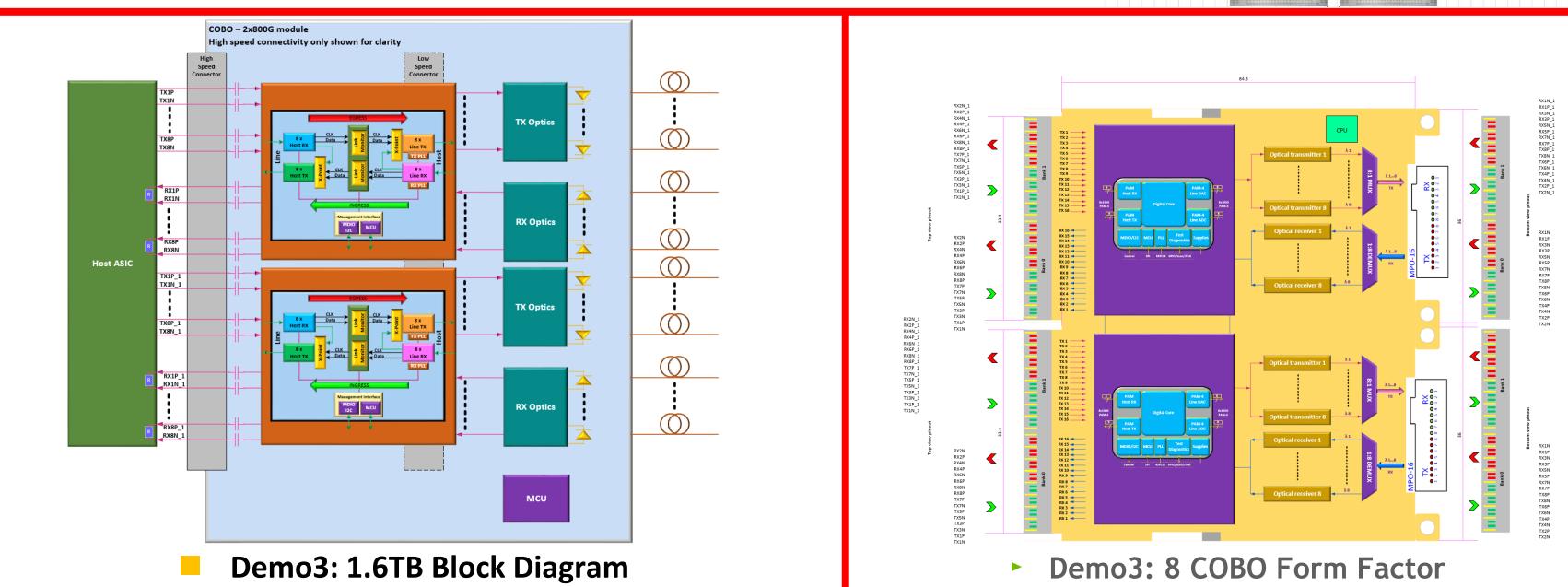


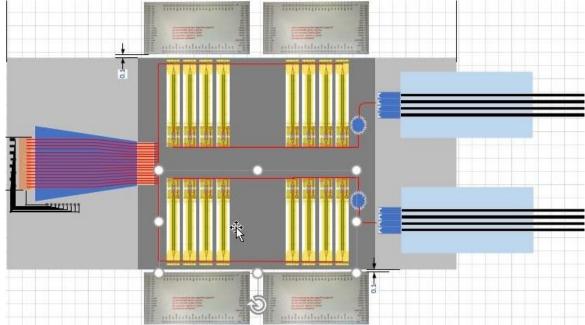




MASSTART PROTOTYPE 3 1.6T 16-lane transceiver

- 16x 100 Gb/s PAM4 optical lanes
- LAN WDM optics (800 GHz): 2x 8λ grid
- **Focus on scalability: WAFT interface for dense optical I/Os**
- **EVB test platform RF Fan-Out**

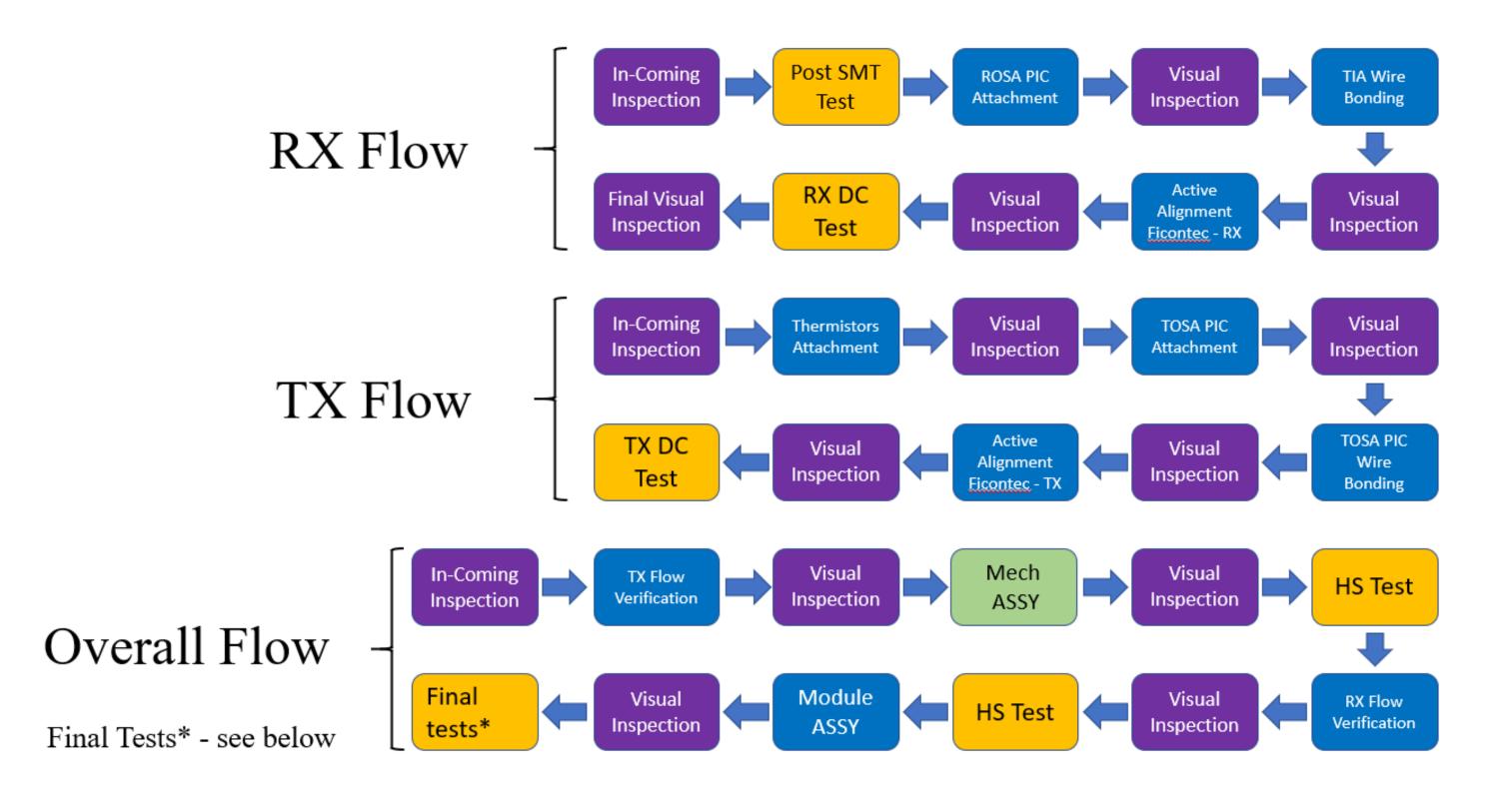




RX1N_1 RX1P_1 RX3N_1 RX5P_1 RX5P_1 RX5P_1 RX5P_1 TX8P_1 TX8P_1 TX8P_1 TX8P_1 TX8P_1 TX8P_1 TX8P_1 TX4P_1 TX4P_1 TX4P_1 TX4P_1 TX2P_1



ASSEMBLY FLOW FOR MASS PRODUCTION





CONCLUSIONS

- Silicon photonics becoming increasingly relevant for short-reach low-cost transceivers
- **Dramatic reductions in assembly and packaging cost needed to meet targets**
- MASSTART is developing an end-to-end solution for mass-manufacturable SiPh transceivers
- MASSTART demonstrators validate the technology in broad deployment scenarios
 - 400G pluggable transceiver
 - **800G EVB for pluggable / on-board optics**
 - 1.6T EVB for on-board / co-packaged optics



ACKNOWLEDGEMENTS





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